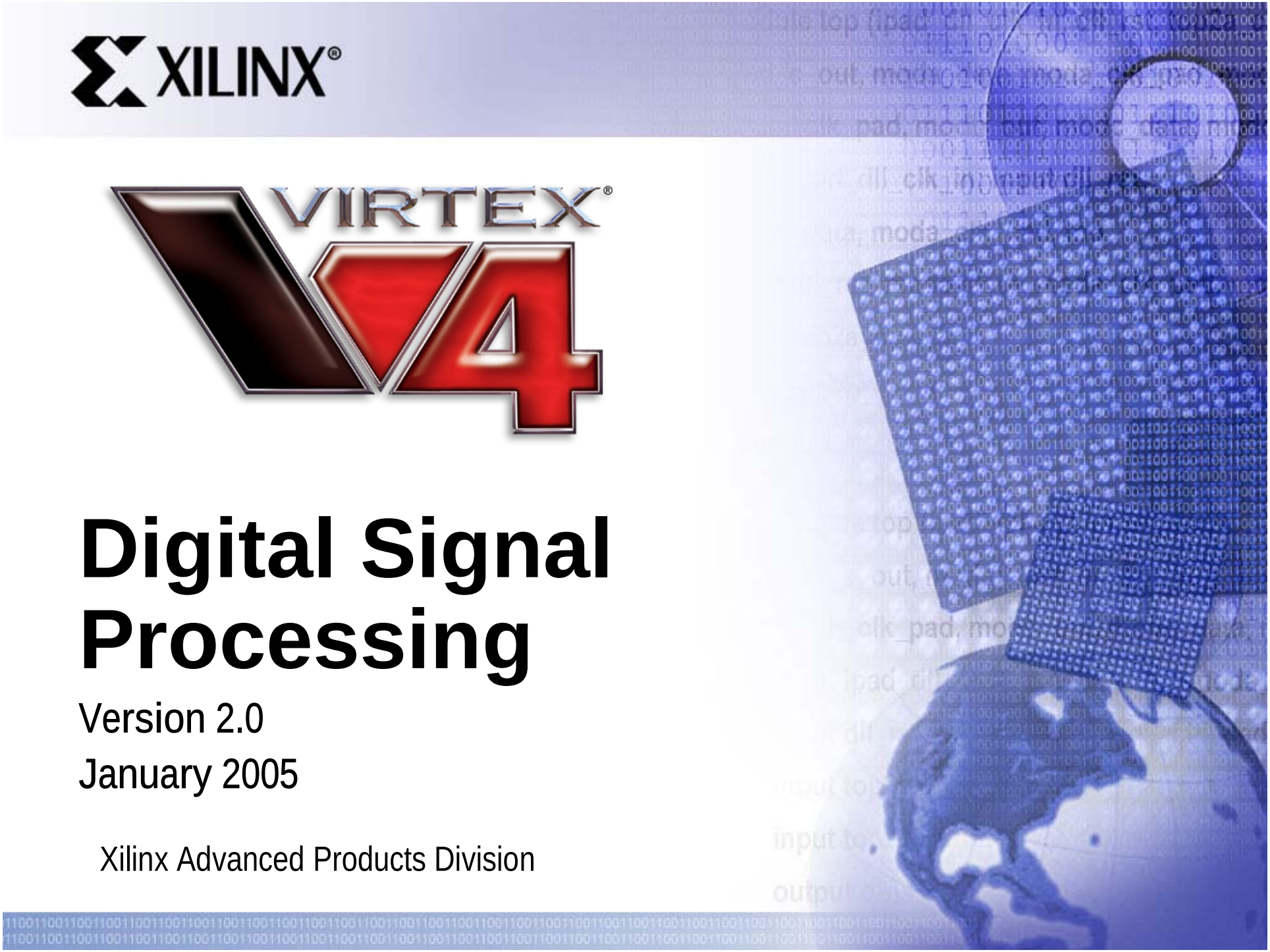



# Digital Signal Processing

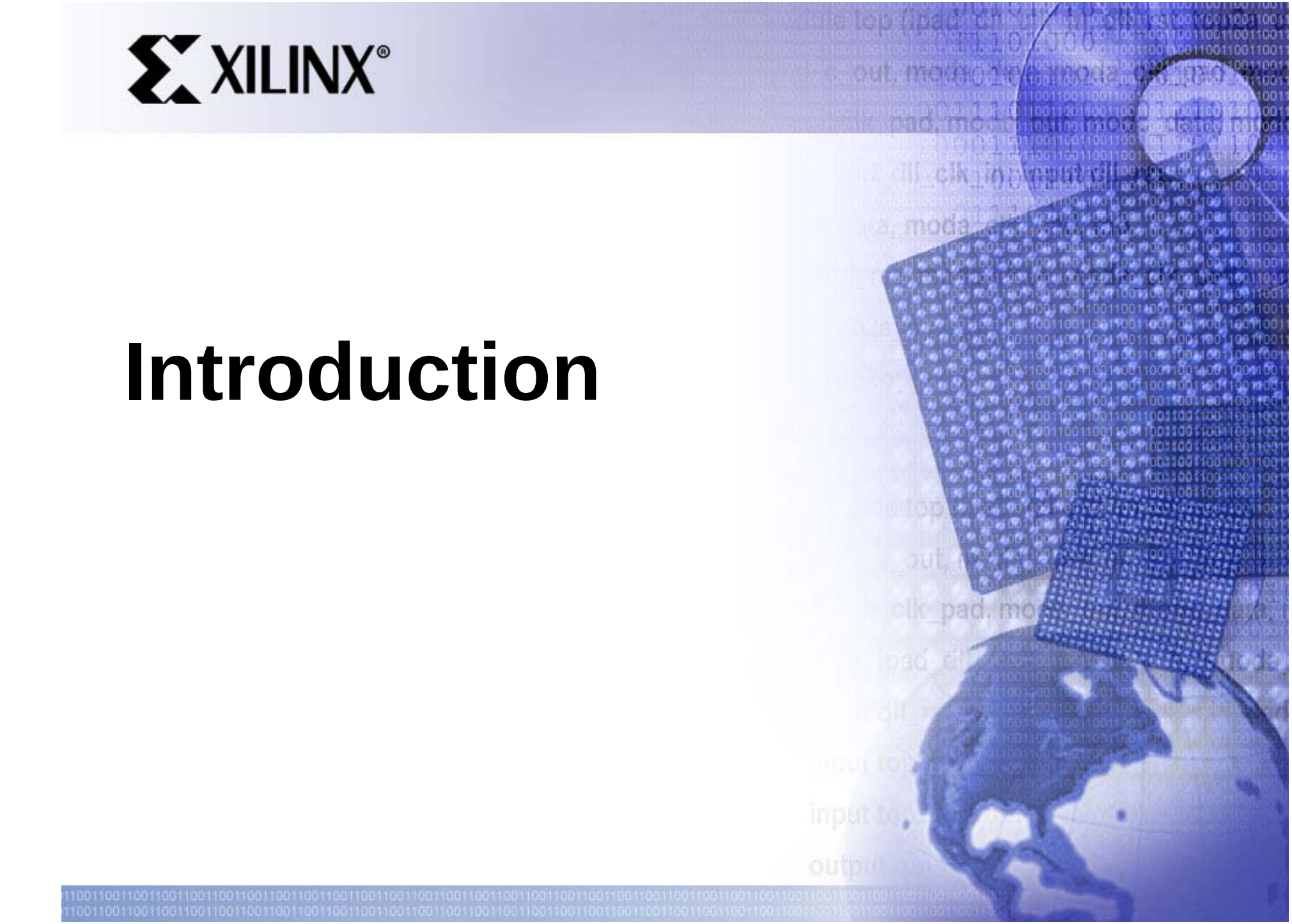
Version 2.0

January 2005

Xilinx Advanced Products Division

# Agenda

- Introduction
- Background
- Virtex-4 Solutions
- Summary



# Introduction

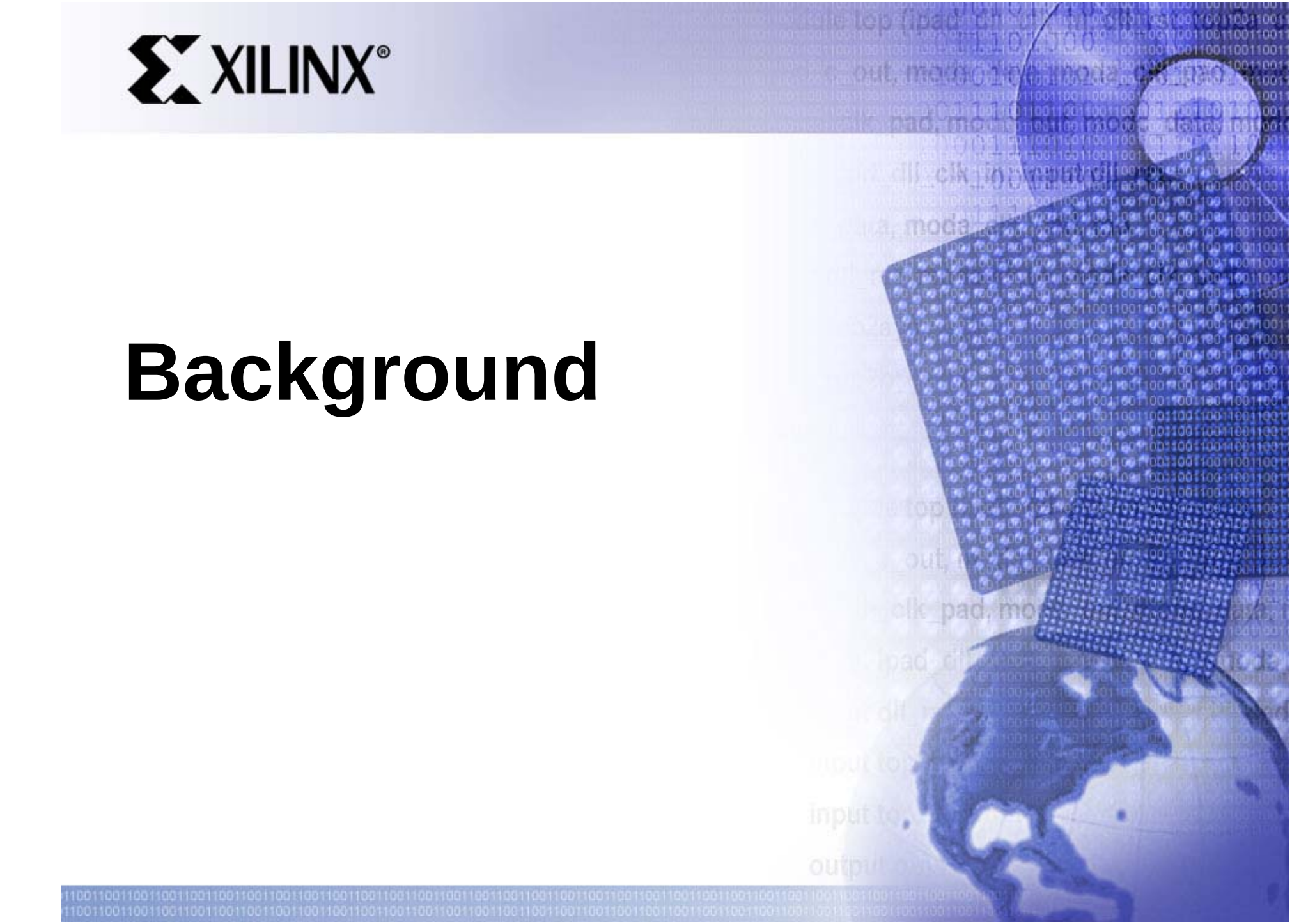
# High-Speed DSP Challenges

- High performance digital communication and video imaging designs challenge existing DSP solutions
  - Need higher performance
  - Need lower costs
  - Need lower power
- Compromises are often made…
  - Performance is sacrificed
  - Time is spent designing substitute implementations

# Achieve DSP Performance and Efficiency in Virtex-4

- Virtex-4 XtremeDSP
  - Performance
    - 512 XtremeDSP slices at 500MHz
    - 256 GMACs/s DSP bandwidth
  - Low Power
    - 2.3mW/100MHz scalable power efficiency
  - Value
    - Operate the XtremeDSP slice in over 40 different modes
    - Highest DSP bandwidth per dollar solution

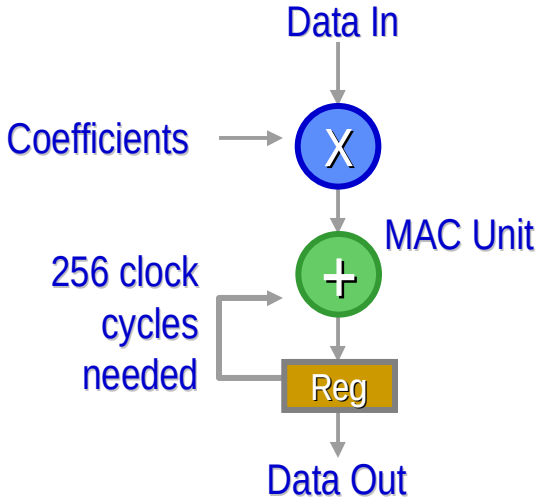

# Background



# FPGAs Enable Massively Parallel DSP

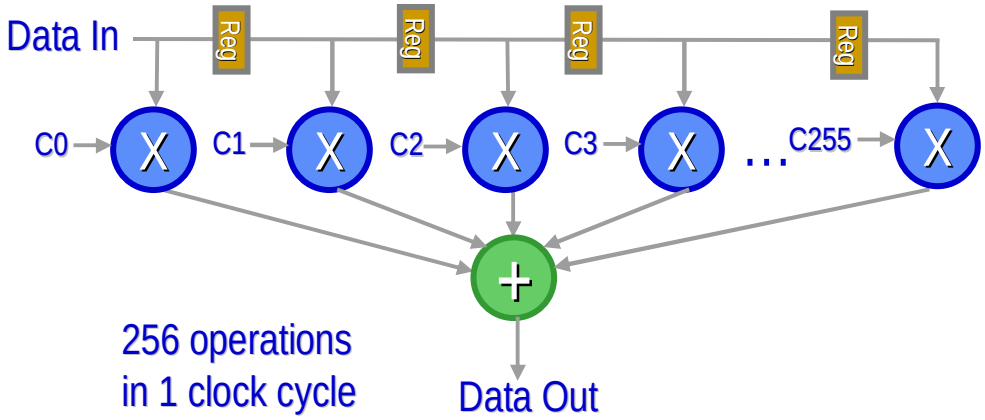
*Example 256 TAP Filter Implementation*

## Programmable DSP - Sequential




$$\frac{1\ GHz}{256\ clock\ cycles} = 4\ MSPS$$

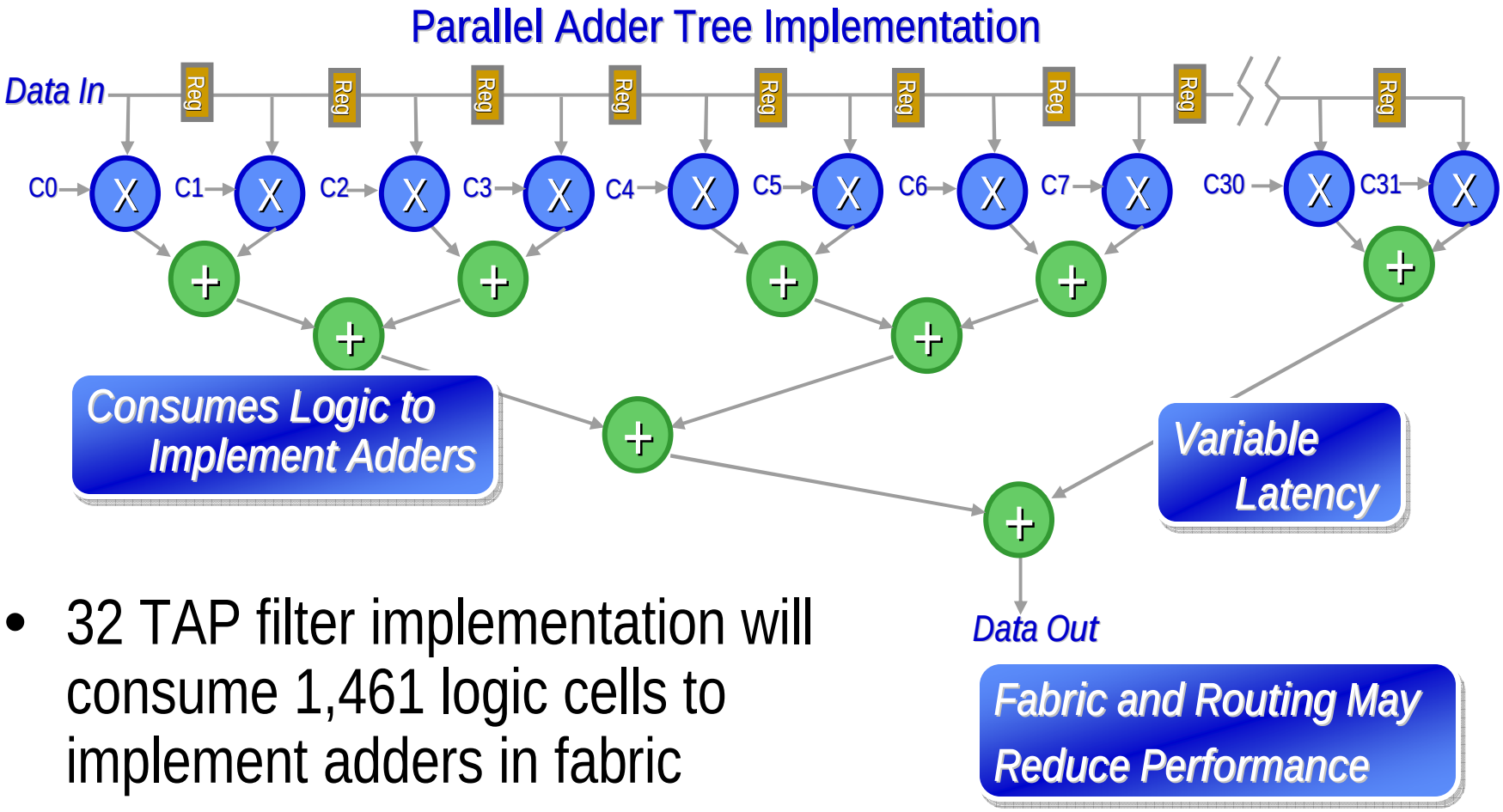
## FPGA - Fully Parallel Implementation




$$\frac{500\ MHz}{1\ clock\ cycle} = 500\ MSPS$$

**"… the unprecedented signal processing requirements of next-generation wireless devices threaten to outpace the capabilities of DSP processors, creating opportunities for massively parallel and highly customized devices." BDTI, 2004**

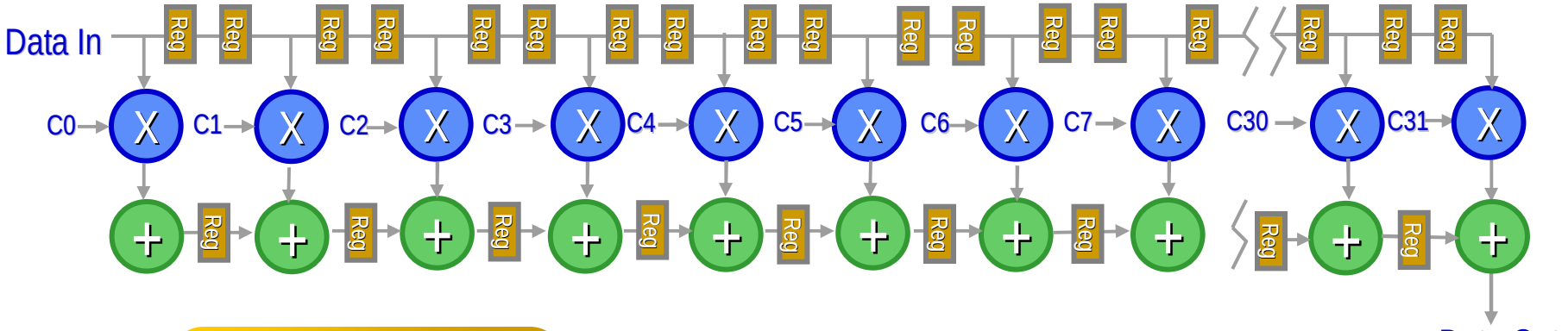
# Parallel Adder Tree Implementation Consumes FPGA resources




- 32 TAP filter implementation will consume 1,461 logic cells to implement adders in fabric

# Virtex-4 Parallel Implementation Consumes Zero Logic Resources

Parallel Adder Cascade Implementation

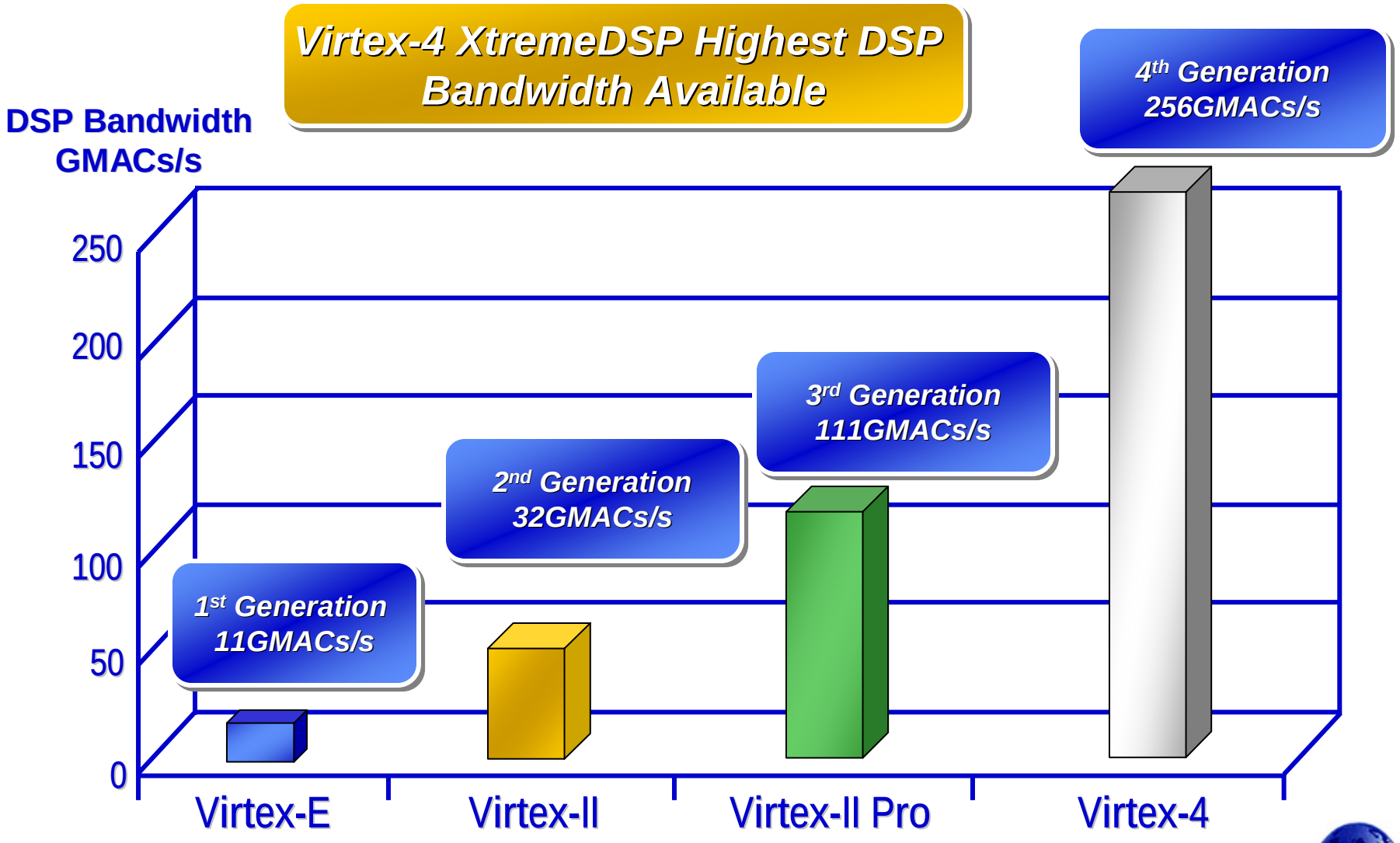



*Filters Implemented Entirely Within the XtremeDSP Slice*

*Guaranteed 500MHz Performance Regardless of Filter Size*

- 32 TAP filter implementation using 32 XtremeDSP Slices

# Xilinx 4th Generation XtremeDSP

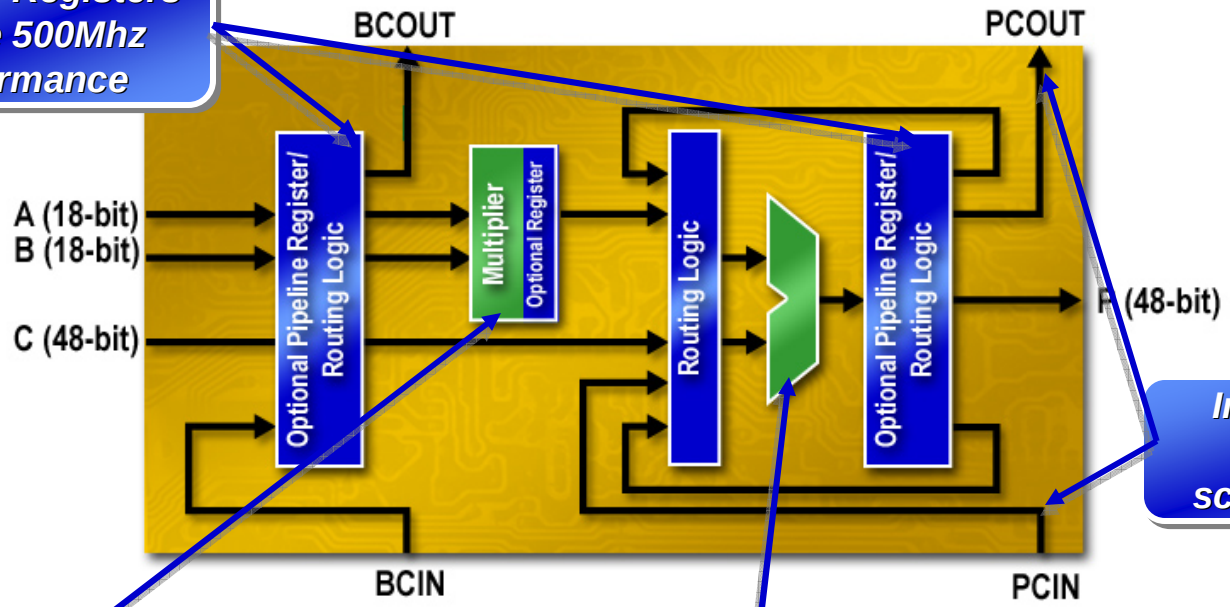


# Virtex-4 Solutions

# Full Custom Design Results in Higher Performance

*Scalable 500MHz performance is impossible with Standard Cell libraries and Standard Cell design flow*

*Pipeline Registers enable 500Mhz performance*




*Integrated Cascade Routing enables scalable performance*

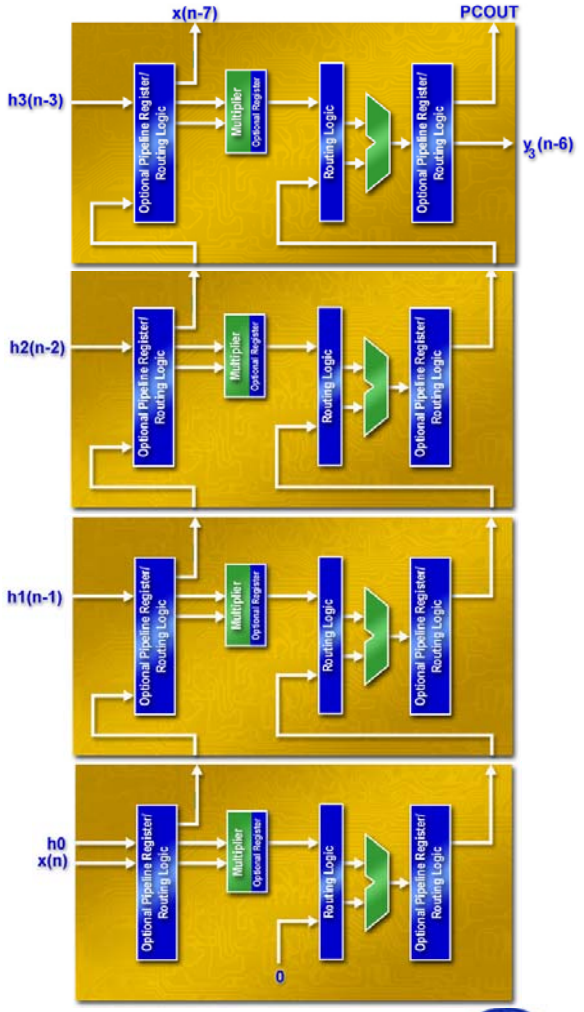
*Arithmatica™ Parallel Counter 20% faster performance and uses less area*

*Arithmatica™ A+Adder 20% faster than other implementations*

*2X the performance of Virtex-II Pro*

# Wide Filters At Full Speed
## Within the Virtex-4 DSP Slice Column

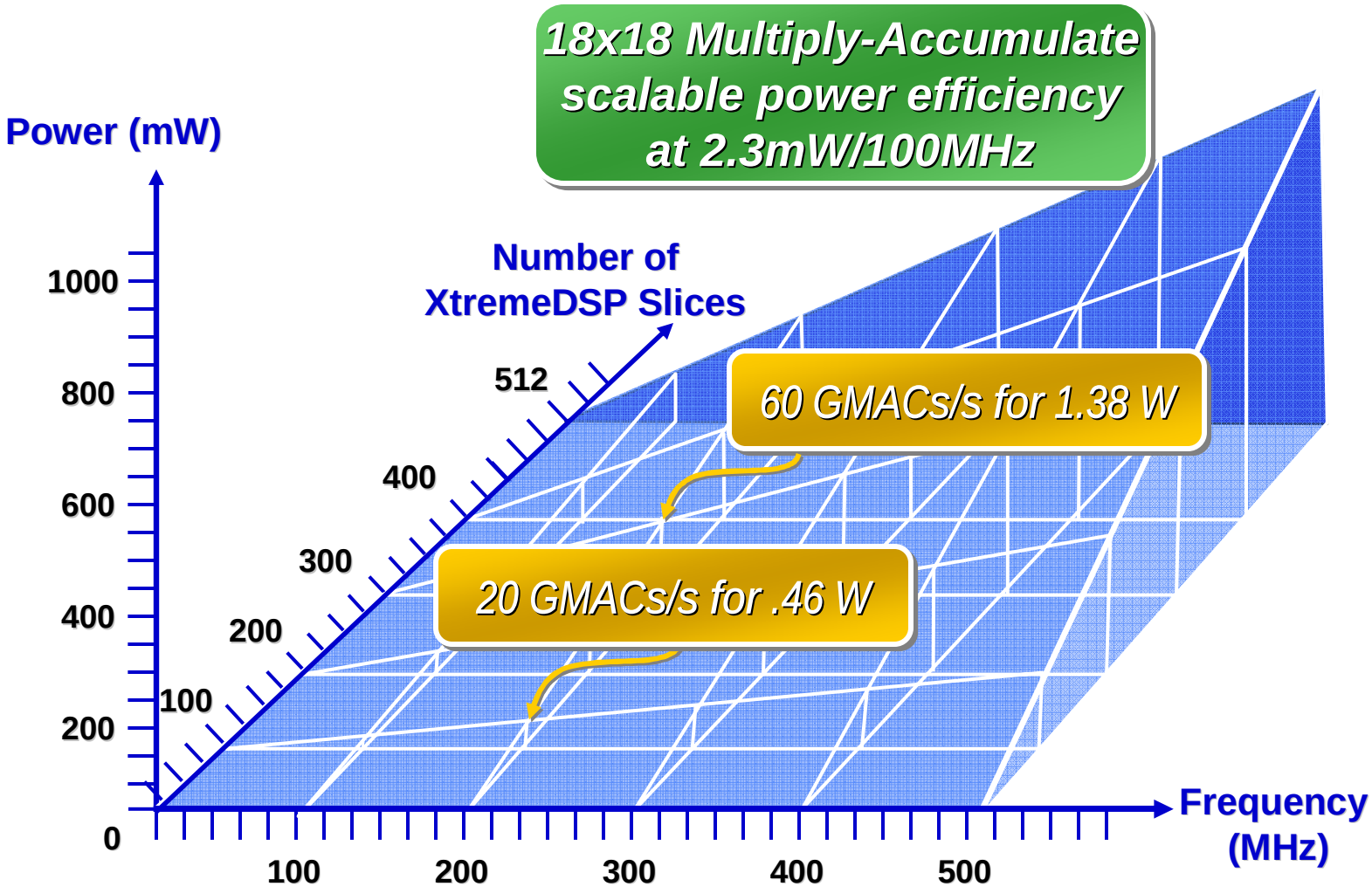
- Systolic N-tap FIR
  - Scalable N-level deep implementation
  - 500MHz performance at N-level deep
- Uses Integrated Pipeline Registers to synchronize filter inputs
- Utilizes Input and Output Cascade Routing




***Build massively parallel 512-TAP FIR filter in a single device achieving 256 GMACs/s performance***

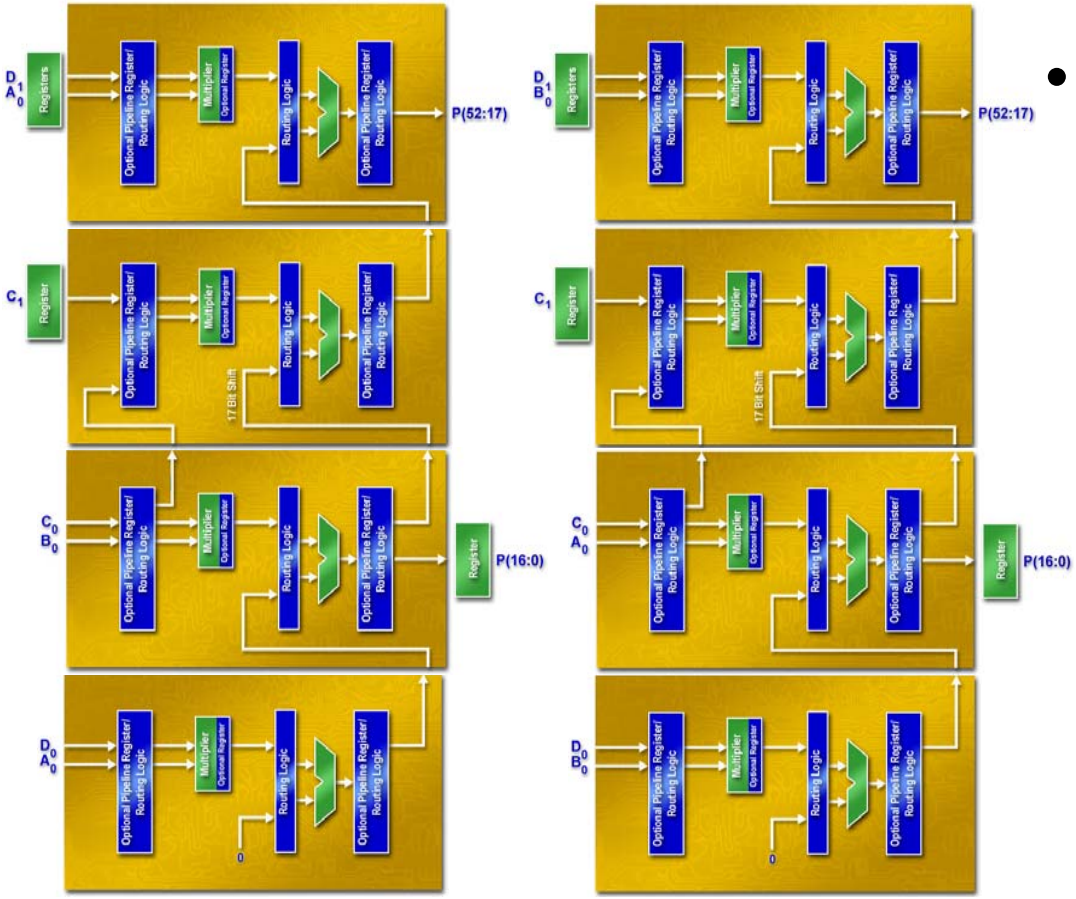
***Equivalent implementation would consume 444 Embedded Multipliers and 77,008 LCs and would only achieve half the performance***

# Lowest Power DSP




Note: Power efficiency achieved using the DSP48 component with a toggle rate of 38%.
It is not an entire MAC with BRAM, control path sequencer/address generator in fabric, and including external routing.

# High-Speed, Low Power Complex Multiply




- Complex filter implementation
  - Register the inputs using minimal external resources
  - Synchronize data using pipeline delay elements

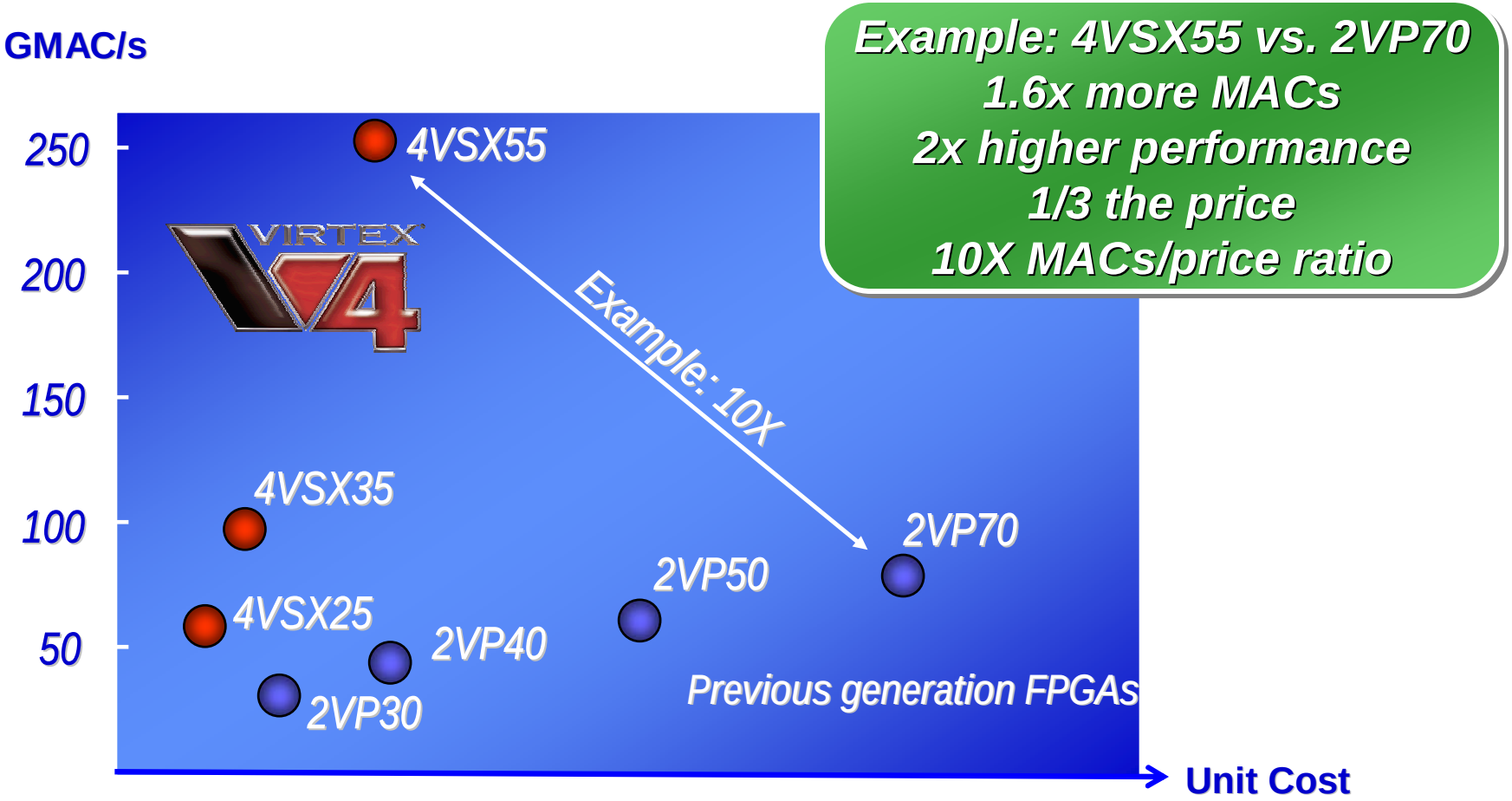
***35x18 Complex Multiply at 500MHz***

***Real and Imaginary 35x18 Complex Multiply consumes only 92mW at 500MHz***

***35x18 Complex Multiply Imaginary Portion***

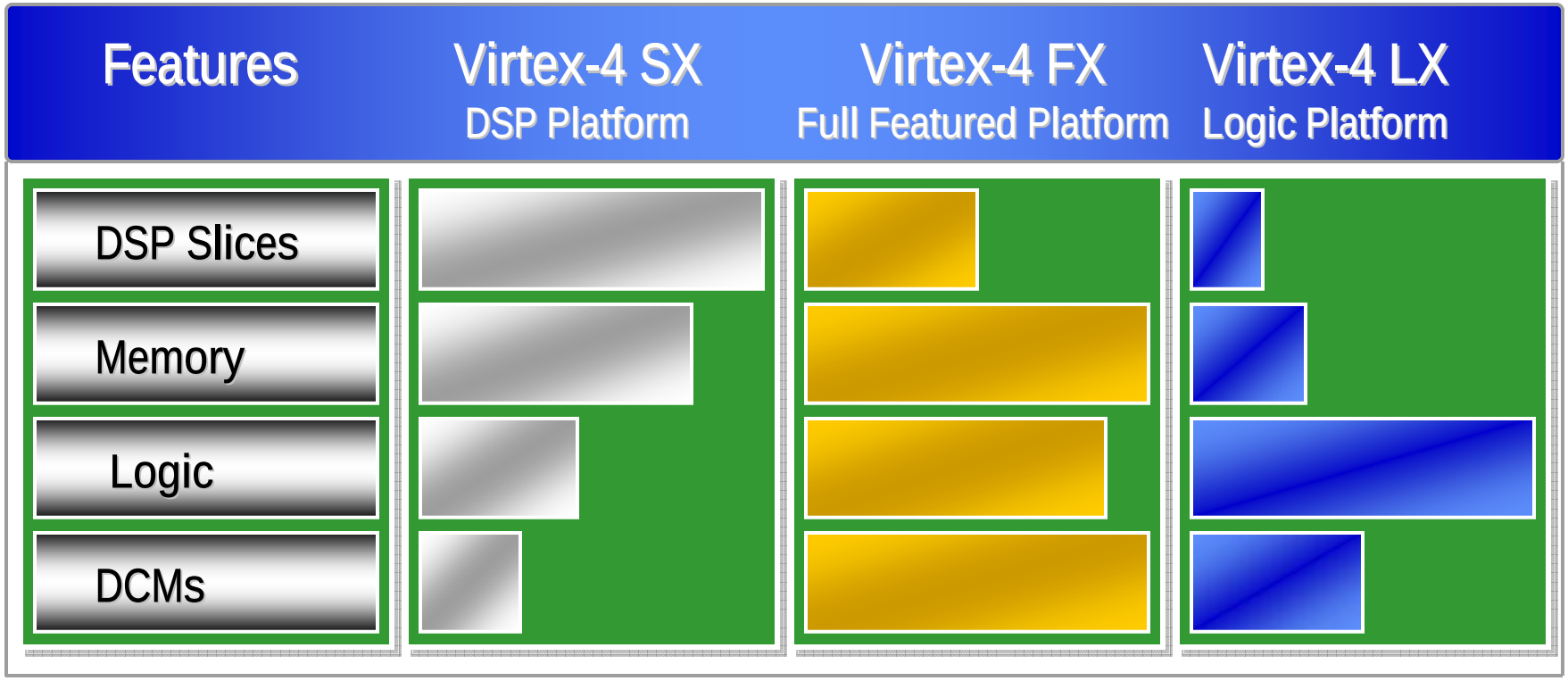
***35x18 Complex Multiply Real Portion***

# Up to 10X Greater DSP Bandwidth Per Dollar




* 18x18 mult. + 48-bit acc.

# Virtex-4 DSP Solutions
## Choose the Right Combination




256GMACs/s
DSP Bandwidth

96GMACs/s
DSP Bandwidth

48GMACs/s
DSP Bandwidth

# Dynamically Programmable DSP Op Modes

| OpMode | Z | | | Y | | X | | Output |
|---|---|---|---|---|---|---|---|---|
| | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Zero | 0 | 0 | 0 | 0 | 0 | 0 | 0 | +/- Cin |
| Hold P | 0 | 0 | 0 | 0 | 0 | 1 | 0 | +/- (P + Cin) |
| A:B Select | 0 | 0 | 0 | 0 | 0 | 1 | 1 | +/- (A:B + Cin) |
| Multiply | 0 | 0 | 0 | 0 | 1 | 0 | 1 | +/- (A * B + Cin) |
| C Select | 0 | 0 | 0 | 1 | 1 | 0 | 0 | +/- (C + Cin) |
| Feedback Add | 0 | 0 | 0 | 1 | 1 | 1 | 0 | +/- (C + P + Cin) |
| 36-Bit Adder | 0 | 0 | 0 | 1 | 1 | 1 | 1 | +/- (A:B + C + Cin) |
| P Cascade Select | 0 | 0 | 1 | 0 | 0 | 0 | 0 | PCIN +/- Cin |
| P Cascade Feedback Add | 0 | 0 | 1 | 0 | 0 | 1 | 0 | PCIN +/- (P + Cin) |
| P Cascade Add | 0 | 0 | 1 | 0 | 0 | 1 | 1 | PCIN +/- (A:B + Cin) |
| P Cascade Multiply Add | 0 | 0 | 1 | 0 | 1 | 0 | 1 | PCIN +/- (A * B + Cin) |
| P Cascade Add | 0 | 0 | 1 | 1 | 1 | 0 | 0 | PCIN +/- (C + Cin) |
| P Cascade Feedback Add Ad | 0 | 0 | 1 | 1 | 1 | 1 | 0 | PCIN +/- (C + P + Cin) |
| P Cascade Add Add | 0 | 0 | 1 | 1 | 1 | 1 | 1 | PCIN +/- (A:B + C + Cin) |
| Hold P | 0 | 1 | 0 | 0 | 0 | 0 | 0 | P +/- Cin |
| Double Feedback Add | 0 | 1 | 0 | 0 | 0 | 1 | 0 | P +/- (P + Cin) |
| Feedback Add | 0 | 1 | 0 | 0 | 0 | 1 | 1 | P +/- (A:B + Cin) |
| Multiply-Accumulate | 0 | 1 | 0 | 0 | 1 | 0 | 1 | P +/- (A * B + Cin) |
| Feedback Add | 0 | 1 | 0 | 1 | 1 | 0 | 0 | P +/- (C + Cin) |
| Double Feedback Add | 0 | 1 | 0 | 1 | 1 | 1 | 0 | P +/- (C + P + Cin) |
| Feedback Add Add | 0 | 1 | 0 | 1 | 1 | 1 | 1 | P +/- (A:B + C + Cin) |
| C Select | 0 | 1 | 1 | 0 | 0 | 0 | 0 | C +/- Cin |
| Feedback Add | 0 | 1 | 1 | 0 | 0 | 1 | 0 | C +/- (P + Cin) |
| 36-Bit Adder | 0 | 1 | 1 | 0 | 0 | 1 | 1 | C +/- (A:B + Cin) |
| Multiply-Add | 0 | 1 | 1 | 0 | 1 | 0 | 1 | C +/- (A * B + Cin) |
| Double | 0 | 1 | 1 | 1 | 1 | 0 | 0 | C +/- (C + Cin) |
| Double Add Feedback Add | 0 | 1 | 1 | 1 | 1 | 1 | 0 | C +/- (C + P + Cin) |
| Double Add | 0 | 1 | 1 | 1 | 1 | 1 | 1 | C +/- (A:B + C + Cin) |

- Enables time-division multiplexing for DSP
- Over 40 different modes
- Each XtremeDSP Slice individually controllable
- Change operation in a single clock cycle
- Control functionality from logic, memory or processor

# Virtex-4 XtremeDSP Slices Useful For More Than DSP

- 6:1 high-speed, 36-bit Multiplexer
  - Use four XtremeDSP Slice and op-modes
  - 500 MHz performance using no programmable logic
    - Save 1584 LCs to build equivalent function in logic
- Dynamic 18-bit Barrel Shifter
  - Use two XtremeDSP slices
  - Use dedicated cascade routing and integrated 17-bit shift
    - Save 1449 LCs to build equivalent function in logic
- 36-bit Loadable Counter
  - Use a single XtremeDSP slice, achieve 500 MHz performance
    - Save 540 LCs to build equivalent function in logic

# XtremeDSP

## FPGAs with DSP Functions


*256 GMACs Performance*


*Lowest Cost (90nm)*

## Shortest Design Time

XILINX SYSTEM GENERATOR™ For DSP


## Major DSP Alliances



## 60+ Advanced DSP Cores

- Comprehensive Library
- Fast Turnaround
- Exceptional Performance

## 60+ DSP Development Boards



## Dedicated Field Specialists

**50+ Field DSP Experts**

## DSP Design Services, Training & Hotline

Distributor Services & Training


- Xilinx Design Services, Education and Support

## Systems Expertise

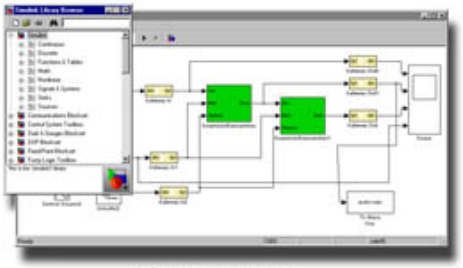
**DSP Division Experts**
- **Tools, IP Solutions**

# Xilinx FPGA DSP Design Flow

FPGA Designer and System Architect

Implement In Hardware

Specify Design



SIMULINK

XILINX SYSTEM GENERATOR™ For DSP

Synthesize Design

VHDL and Coregen Output

```
ENTITY parityFunction IS
      PORT( A,B,C : IN t_wlogic; parity : OUT t_wlogic )
END parityFunction;
ARCHITECTURE full OF parityFunction IS
BEGIN
      PROCESS (A, B, C)
            VARIABLE count : integer;
            BEGIN
                  count := 0;
                  IF A = '1' THEN count := count +1; END IF;
                  IF B = '1' THEN count := count +1; END IF;
                  IF C = '1' THEN count := count +1; END IF;
                  IF (count MOD 2) = 0 THEN
                        OUT <= '0';
                  ELSE
                        OUT <= '1';
                  END IF;
      END PROCESS;
END full;
```

ISE ALL THE SPEED YOU NEED

DSP Architectural Wizard

# Summary

# Virtex-4 XtremeDSP

- Enabling next generation high-performance DSP
  - Highest Performance
    - 512 XtremeDSP slices at 500MHz
    - 256 GMACs/s DSP bandwidth
  - Lowest Power
    - 2.3mW/100MHz
  - Most Value
    - Operate the XtremeDSP slice in over 40 different modes
    - Highest DSP bandwidth per dollar solution available

# If You Want to Learn More…

- Evaluate XtremeDSP in Virtex-4
  - Request an advanced DSP presentation
    - Learn about advanced, high performance filter implementations only possible in Virtex-4
  - Request a demo of the new XtremeDSP capability in Virtex-4 today
    - See the fastest, lowest power FPGA DSP solution available
  - Visit www.xilinx.com/dsp for more information on Xilinx DSP solutions