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Project Name: xsocVGAStripes

Creation Date: July 2003
Development Board: XESS XSA-100 Plus XStend Version 2
Development Software: Xilinx ISE Version 5.1.03i

Description

This project generates a vga signal and displays a set of monochrome bars on a monitor. The project uses the vga circuit design provided in Jan Gray's XSOC project (see references). Basically is generates the correct timing signals needed and shifts through a 16-bit word one bit at a time (monochrome) for pixel information.

This project demonstrates how to mix both VHDL and Verilog code together.

The XStend board is not required in this project.

The XSA-100 board frequency must be set to 12.5 MHz!

Note: The vga circuit as provided in the XSOC project has a bug. It reads 576x455 bits of data for image display, but only displays 560x455. The last 16-bit word of pixel data read for display on each horizontal line is not displayed. In other words, the right side of the image is cut off. This problem has been corrected in the version supplied.

Project Directory Structure

This project is organized into the following directories:

./ - contains all the files need to synthesize the design.

./config – effectively a backup of all main files in the root directory

./docs – this PDF file. Source files used to build this PDF are located in ./docs/src.

./src – source directory for all HDL files

./temp – temporary directory used during the build process.

Synthesis

The project is built and maintained using two windows based batch files. The first is "make.bat". It simply issues are the commands required to "compile" all the source files in the ./src directory and eventually generate the chipIO.bit file to downloaded to the fpga.

The second batch file is called "clean.bat". Its sole purpose is to delete most of the unwanted files generated during the build process.

References

The primary reference for building this project is Jan Gray's XSOC project. This project is an excellent place to start on how to build a fully pipelined risc based cpu interfaced with a video display and other devices. See the www.fpgacpu.org website for the complete XSOC project and information.