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Project Name: timerIO

Creation Date: June 2003
Development Board: XESS XSA-100 Plus XStend Version 2
Development Software: Xilinx ISE Version 5.1.03i

Description

This is a good introductory project for a new owner of an XSA-100 board and in general, fpga programming. It demonstrates several things. First, how to setup a project that needs to interface to the outside world through the fpga chip's I/O pins. A top level VHDL entity called chipIO provides this interface. I/O pins for accessing the push button and for driving the 7-segment led display are declared in the chipIO entity and specified in the ucf file.

Secondly, this project demonstrates one way to create a simple timer by counting clock cycles. Approximately each second the value displayed on the 7-segment display is incremented. The design resets if the push button is pressed.

The XStend board is not required in this project.

The XSA-100 board frequency must be set to 5 MHz!

Project Directory Structure

This project is organized into the following directories:

./ - contains all the files need to synthesize the design.

./config – effectively a backup of all main files in the root directory

./docs – this PDF file. Source files used to build this PDF are located in ./docs/src.

./src – source directory for all HDL files

./temp – temporary directory used during the build process.

Synthesis

The project is built and maintained using two windows based batch files. The first is "make.bat". It simply issues are the commands required to "compile" all the source files in the ./src directory and eventually generate the chipIO.bit file to downloaded to the fpga.

The second batch file is called "clean.bat". Its sole purpose is to delete most of the unwanted files generated during the build process.