GTIA

C014805 (NTSC)

CONFIDENTIAL

REVISIONS			
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QUALITY ASSURANCE

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TITLE

GTIA CHIP (NTSC)

SIZE	DRAWING NO.	REV
A	C014805	A

SCALE -

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1.0) GENERAL:

The GTIA performs color-luminance control, player-missile control, priority control, collision detection, and miscellaneous I/O functions.

There are nine color-luminance registers. There is one color-luminance register for each player-missile, playfield type and background. When two or more color-luminance overlap there must be a decision made as to which object will have priority. This is done by hardware with a priority register to select which group of objects have priority over other objects.

The GTIA has a horizontal position register for each player and missile. It also has a size control register for each player and a single graphic register for the missiles. There is a graphics register for each player and a single register for the missiles. There is collision detect between all players, missiles, and playfield. However, there is no collision detect between each playfield.

There are four trigger inputs and four bi-directional I/O pins for miscellaneous I/O functions. There are three inputs that receive data from the ANTIC to generate the playfield graphics and syncs the GTIA with the ANTIC.

2.0) COLOR-LUMINANCE CONTROL

A color-luminance register is used on the GTIA chip for each player-missile and playfield type. Each color-luminance register is loaded by the microprocessor with a code representing the desired color and luminance of its corresponding player-missile or playfield type. As the serial data of the different objects pass through the GTIA, it is "impressed" with the color and luminance values in these registers. Therefore, when a player, missile, or playfield is turned on, the corresponding color and luminance will be turned on. To prevent two color-luminance from fighting, priority is established. (See section 3.0 for Priority).

2.0) COLOR-LUMINANCE CONTROL (Continued):

THESE ADDRESSES WRITE DATA TO THE FOLLOWING REGISTERS:

COLOR-LUM OF PLAYER-MISSILE 0 (COLPM0) ADDR. = 12
COLOR-LUM OF PLAYER-MISSILE 1 (COLPM1) ADDR. = 13
COLOR-LUM OF PLAYER-MISSILE 2 (COLPM2) ADDR. = 14
COLOR-LUM OF PLAYER-MISSILE 3 (COLPM3) ADDR. = 15

COLOR-LUM OF PLAYFIELD 0 (COLPF0) ADDR. = 16
COLOR-LUM OF PLAYFIELD 1 (COLPF1) ADDR. = 17
COLOR-LUM OF PLAYFIELD 2 (COLPF2) ADDR. = 18
COLOR-LUM OF PLAYFIELD 3 (COLPF3) ADDR. = 19

COLOR-LUM OF BACKGROUND (COLBK) ADDR. = 1A

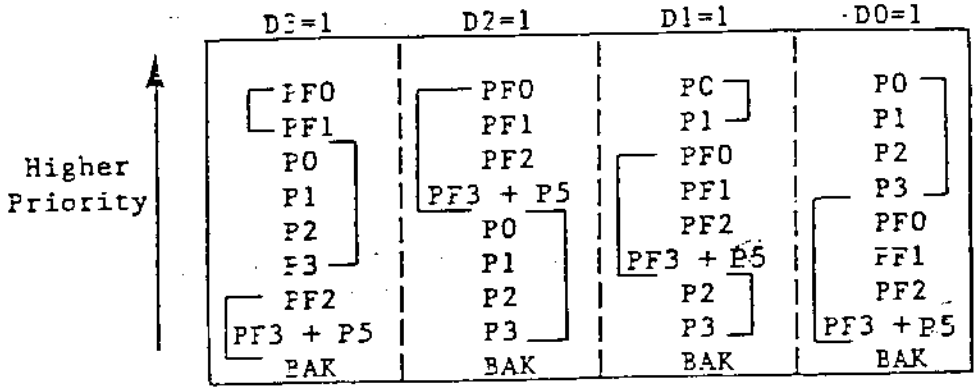
Color				Luminance			Not Used	
D7	D6	D5	D4	D3	D2	D1		
X	X	X	X	0	0	0		Zero Luminance (black)
				0	0	1		
					ETC.			
				1	1	1		Max. Luminance (white)
0	0	0	0	Grey				
0	0	0	1	Gold				
0	0	1	0	Orange				
0	0	1	1	Red-Orange				
0	1	0	0	Pink				
0	1	0	1	Purple				
0	1	1	0	Purple-Blue				
0	1	1	1	Blue				
1	0	0	0	Blue				
1	0	0	1	Light-Blue				
1	0	1	0	Turquoise				
1	0	1	1	Green-Blue				
1	1	0	0	Green				
1	1	0	1	Yellow-Green				
1	1	1	0	Orange-Green				
1	1	1	1	Light-Orange				

3.0) PRIORITY CONTROL:

Priority (PRIOR) ADDR. = 1B

When moving objects such as players, missiles and playfield overlap on the TV screen, a decision must be made as to which object shows in front of the other. Objects which appear to pass in front of other objects are said to have priority over them. Priority is assigned to each object by the GTIA chip before the serial data from each object is combined with the other chip before the serial data from each object is combined with the other objects and sent out to the TV screen. Setting the priority is done by writing from the microprocessor to the GTIA priority control control register (PRIOR).

D3, D2, D1, & D0 — Priority Select (Mutually Exclusive). These bits select one of 4 types of priority. Objects with higher priority will appear to move in front of objects with lower priority.



NOTE: The use of Priority bits in a "non-exclusive" mode (more than 1 bit true) will result in objects (whose priorities are in conflict) turning BLACK in the overlap region.

EXAMPLE: PRIOR code = 1010 This will black P0 or P1 if they are over PF0 or PF1. It will also black P2 or P3 if they are over PF2 or PF3.

The priority control register also controls the fifth player. The fifth player is the combination of all four missiles and shown as playfield 3 color-lum. However, there is no priority between playfields. Therefore, the fifth player would have no priority between playfields.

D4 Fifth Player Enable

This bit causes all missiles to assume the color of Playfield Type 3. (COLPF3). This allows missiles to be positioned together with a common color for use as a fifth player.

The priority control register also controls multiple color players. When enabled, the color-lum of player-missile 0 and player-missile 1 is to be logically "ORed". Also the color-lum of player-missile 2 and player-missile 3 is to be logically "ORed". This permits overlapping of the position of two players with the choice of a third color in the overlapped region.

D5 Multiple Color Player Enable.

This bit causes the logical "or" function of the bits of the colors of Player 0 with Player 1, and also of Player 2 with Player 3. This permits overlapping the position of 2 players with a third color in the overlapped region.

The priority control register also controls playfield data interpretation from the ANTIC. There are four modes. They are 4 color-lum (normal CTIA mode), 1 color-16 lum (GTIA), 9 color-lum (GTIA), and 16 color-lum (GTIA).

D7 & D6 GTIA PLAYFIELD MODES

D7	D6	OPTIONS
0	0	NORMAL No GTIA mode (CTIA operation)
0	1	1 COLOR - 16 LUMINANCES MOCE
1	0	9 COLOR-LUMINANCES MODE
1	1	16 COLOR - 1 LUMINANCE MODE

3.0) PRIORITY CONTROL (continued):

In the normal mode, the GTIA will interpret the AN0-AN2 data from ANTIC as:

AN2	AN1	AN0	
0	0	0	: background color
0	0	1	: vertical sync
0	1	0	: horizontal blank and clear 40 character mode
0	1	1	: horizontal blank and set 40 character mode
1	0	0	: playfield 0
1	0	1	: playfield 1
1	1	0	: playfield 2
1	1	1	: playfield 3

Refer to the ANTIC data sheet for normal ANTIC display of playfield.

NOTE: If the GTIA is in the 40 character mode, there is no priority between playfield 1 luminance and all player-missile luminances.

In the 1 color - 16 lums mode, the GTIA will interpret the AN0-AN2 from the ANTIC as:

AN2	AN1	AN0	
0	0	0	: background color
0	0	1	: vertical sync
0	1	0	: horizontal blank and clear 40 character mode
0	1	1	: horizontal blank and set 40 character mode
1	D3	D2	: LUM D3 D2 of LUM D3 D2 D1 D0
1	D1	D0	: LUM D1 D0 of LUM D3 D2 D1 D0

NOTE: Dn indicates data

In the 16 lum mode, it takes 2 color clocks to make one playfield pixel. The ANTIC will send the AN2 to AN0 data every color clock. At the beginning of a pixel, lum D3 and lum D2 are loaded for the next pixel and on the second color clock, lum D1 and lum D0 are loaded for the next pixel. The background color register is used for the playfield color and the background lum register is "ORed" with lum D3 D2 D1 D0 for playfield luminance. Therefore, zero should be loaded into background luminance in this mode.

3.0) PRIORITY CONTROL (continued):

In the 9 color-lum mode, the GTIA will interpret the AN0-AN2 from the ANTIC as:

A N Z 2	A N 1	A N 0	
0	0	0	: background color
0	0	1	: vertical sync
0	1	0	: horizonal blank and clear 40 character mode
0	1	1	: horizonal blank and set 40 character mode
1	D3	D2	: DATA D3 D2 of DATA D3 D2 D1 D0
1	D1	D0	: DATA D1 D0 of DATA D3 D2 D1 D0

NOTE: Dn indicates data

In the 9 color-lum mode, it takes 2 color clocks to make one playfield pixel. The ANTIC will send the AN2 to AN0 data every color clock. At the beginning of a pixwl, data D3 and data D2 are loaded for the next pixel and on the second color clock, data D1 and data D0 are loaded for the next pixel. The data word D3 to D0 determines one of the nine color-lum registers for that pixel. (See table below for data to color register assignment.)

D 3	D 2	D 1	D 0	DATA
0	0	0	0	: COLOR-LUM OF PLAYER-MISSILE 0
0	0	0	1	: COLOR-LUM OF PLAYER-MISSILE 1
0	0	1	0	: COLOR-LUM OF PLAYER-MISSILE 2
0	0	1	1	: COLOR-LUM OF PLAYER-MISSILE 3
X	1	0	0	: COLOR-LUM OF PLAYFIELD 0
X	1	0	1	: COLOR-LUM OF PLAYFIELD 1
X	1	1	0	: COLOR-LUM OF PLAYFIELD 2
X	1	1	1	: COLOR-LUM OF PLAYFIELD 3
1	0	X	X	: COLOR-LUM OF BACKGROUND

NOTE: X INDICATES "DON'T CARES"

3.0) PRIORITY CONTROL (continued):

In the 16 color - 1 lums mode, the GTIA will interpret the AN0-AN2 from the ANTIC as:

AN2	AN1	AN0	
0	0	0	: background color
0	0	1	: vertical sync
0	1	0	: horizonal blank and clear 40 character mode
0	1	1	: horizonal blank and set 40 character mode
1	D3	D2	: COLOR D3 D2 of COLOR D3 D2 D1 D0
1	D1	D0	: COLOR D1 D0 of COLOR D3 D2 D1 D0

NOTE: Dn indicates data

In the 16 color mode, it takes 2 color clocks to make one playfield pixel. The ANTIC will send the AN2 to AN0 data every color clock. At the beginning of a pixel, color D3 and color D2 are loaded for the next pixel and on the second color clock, color D1 and Color D0 are loaded for the next pixel. The background luminance register is used for the playfield luminance and the background color register is "ORed" with color D3 D2 D1 D0 for playfield color. Therefore, zero should be loaded into background color in this mode.

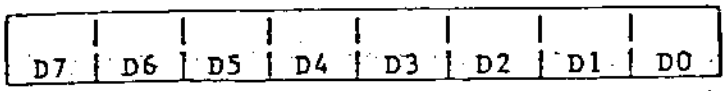
4.0) PLAYER-MISSILE CONTROL:

The players and missiles are small objects which can be moved quickly in the horizontal direction by changing their position registers. They are called players and missiles because they were originally designed to be used in games for objects such as airplanes and bullets. However, there are many other possible applications for them. The four player-missile color registers, in conjunction with the four playfield color registers and the background color register, make it possible to display 9 different colors at the same time.

There are a total of four players and four missiles. The four missiles may be grouped together and used as a 5th player. These objects are positioned horizontally by 8 horizontal position registers (HPOS (X)). These registers may be reloaded at any time hy the processor, allowing an object to be replicated many times across a horizontal TV line.

PLAYER HORIZONTAL POSITION:
HPOSP0 (Player 0) Addr. =00
HPOSP1 (Player 1) Addr. =01
HPOSP2 (Player 2) Addr. =02
HPOSP3 (Player 3) Addr. =03
HPOSM0 (Missile 0) Addr. =04
HPOSM1 (Missile 1) Addr. =05
HPOSM2 (Missile 2) Addr. =06
HPOSM3 (Missile 3) Addr. =07

These addresses write data into the player or missile horizontal position register. The horizontal position value determines the color clock location of the left edge of the object. Hex 30 is the left edge of a standard width screen. Hex D0 is the right edge of a standard screen.



The shape of a player or missile is determined by the data in the graphics register. The players have independent eight bit graphics registers. These registers may also be reloaded at any time by the microprocessor, although they are usually changed during horizontal blank time. The data in these graphic registers is placed on the display whenever the horizontal counter equals the corresponding horizontal

position registers. The same data will be displayed every line unless the graphic registers are reloaded with new data. These player-missile graphic registers may also be reloaded automatically from memory with direct memory access (DMA). To use DMA for the player-missile graphics, $\overline{\text{HALT}}$ input must go low during horizontal blank. From the falling edge of $\overline{\text{HALT}}$, the GTIA will pull the graphic data from the data bus, if they are enabled by GRACTL. However, the GTIA does not address the data. This is done by the ANTIC. Therefore, to DMA player-missile graphic, the GTIA must be used in conjunction with ANTIC. (See the ANTIC data sheet for use of DMA.) DMA timing is shown on next page.

GRACTL (Graphic control register) Addr.=1D

This address writes data to the graphic control register.

Not Used	D2	D1	D0

D2 = 1 Enable latches on TRIG0 – TRIG3 inputs (latches are cleared and TRIG0 – TRIG3 act as normal inputs when this control bit is zero).

D1 = 1 Enable Player DMA to Player Graphics Registers.

D0 = 1 Enable Missile DMA to Missile Graphics Registers.

DMA is enabled by setting both DMACTL (ANTIC) and GRACTL (GTIA). Setting the DMACTL only will result in cycles to be stolen but no display will be generated for players or missiles.

Graphic Register:

GRAFP0 (Player 0 graphic register) Addr.=0D
GRAFP1 (Player 1 graphic register) Addr.=0E
GRAFP2 (Player 2 graphic register) Addr.=0F
GRAFP3 (Player 3 graphic register) Addr.=10

D7	D6	D5	D4	D3	D2	D1	D0

Left Right

Player on TV Screen

GRAFM (Missile graphic register) Addr.=11

D7	D6	D5	D4	D3	D2	D1	D0
L	R	L	R	L	R	L	R
M3		M2		M1		M0	

These addresses write data directly into the player graphic register, independent of DMA. These registers also maybe accessed by DMA.

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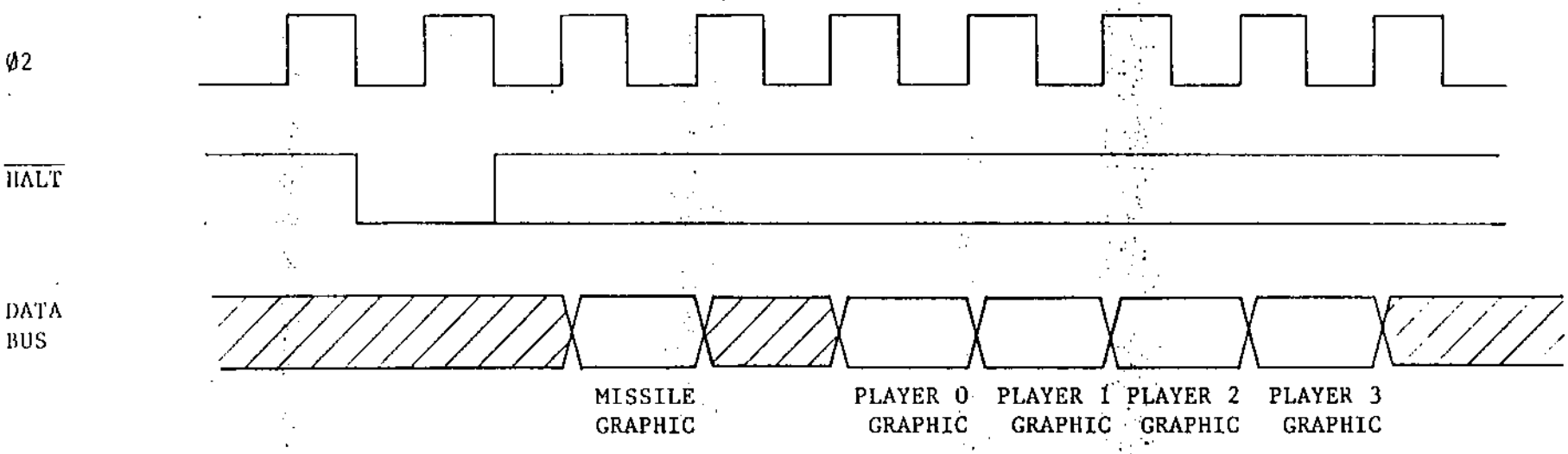
DMA TIMING for GTIA

during horizontal blank



NOTE: GTIA does not address the data but only looks for the data.

4.0) PLAYER-MISSILE CONTROL:

Each player or missile can be delayed by one vertical line. VDELAY is used to give one-line resolution in the vertical positioning of an object when the two-line resolution display is enabled. Setting a bit in VDELAY to a logical one will move the corresponding object down by one TV line.

VDELAY (Vertical delay) Addr.=1C

This address writes data into the vertical delay register.

D7	D6	D5	D4	D3	D2	D1	D0
P3	P2	P1	P0	M3	M2	M1	M0

Each player and missile can be displayed by three different sizes. There is normal, two times normal, and four times normal. Normal size is one color clock per bit in the graphics register.

SIZE REGISTERS:

SIZEP0 (Player 0 size) Addr.=08
SIZEP1 (Player 1 size) Addr.=09
SIZEP2 (Player 2 size) Addr.=0A
SIZEP3 (Player 3 size) Addr.=0B

Not Used	D1	D0	Horizontal Size Register (Player)
	0	0	Normal Size (8 color clocks wide)
	0	1	Twice Normal Size (16 color clocks wide)
	1	0	Normal Size
	1	1	4 Times Normal Size (32 color clocks wide)

SIZEM (All missiles sizes) Addr.=0C

D7	D6	D5	D4	D3	D2	D1	D0	Horizontal Size Register (Missile)
M3		M2		M1		M0		
						0	0	Normal Size (2 color clocks wide)
						0	1	Twice Normal Size (4 color clocks wide)
						1	0	Normal Size
						1	1	4 Times Normal Size (8 color clocks wide)

These addresses write data into the player or missiles control registers.

5.0) COLLISION:

Sixty bits of collision register are provided to detect and store overlap (hits) between players, missiles, and playfield. These collisions can be read by the microprocessor from the addresses 00 through 0F. There are no bits for missile to missile or playfield to playfield collisions. There are sixteen bits for missile to playfield. There are sixteen bits for player to playfield. There are sixteen bits for missile to player. There are twelve bits for player to player because P0 to P0 always read zero, etc.. In the high resolution mode (one pixel per 1/2 color clock), the playfield is represented by playfield 1 luminance and playfield 2 color. In this mode, playfield collision is stored as a playfield 2 collision.

COLLISION REGISTERS:

M0PF (Missile 0 to playfield collisions) Addr.=00
M1PF (Missile 1 to playfield collisions) Addr.=01
M2PF (Missile 2 to playfield collisions) Addr.=02
M3PF (Missile 3 to playfield collisions) Addr.=03

Not Used (zero forced)	D3	D2	D1	D0
	3	2	1	0

Playfield Type

P0PF (Player 0 to playfield collisions) Addr.=04
P1PF (Player 1 to playfield collisions) Addr.=05
P2PF (Player 2 to playfield collisions) Addr.=06
P3PF (Player 3 to playfield collisions) Addr.=07

Not Used (zero forced)	D3	D2	D1	D0
	3	2	1	0

Playfield Type

M0PL (Missile 0 to player collisions) Addr.=08
M1PL (Missile 1 to player collisions) Addr.=09
M2PL (Missile 2 to player collisions) Addr.=0A
M3PL (Missile 3 to player collisions) Addr.=0B

Not Used (zero forced)	D3	D2	D1	D0
	3	2	1	0

Player Number

P0PL (Player 0 to player collisions) Addr.=0C
P1PL (Player 1 to player collisions) Addr.=0D
P2PL (Player 2 to player collisions) Addr.=0E
P3PL (Player 3 to player collisions) Addr.=0F

Not Used (zero forced)	D3	D2	D1	D0
	3	2	1	0

Player Number

These addresses read the collisions registers.

5.0) COLLISION (continued):

These collision registers can be cleared by writing to a single register. All collision registers are cleared when this is done.

HITCLR (Colision "hit" clear) Addr.=1E

Not Used

6.0) NTSC/PAL REGISTER:

There are two versions of the GTIA: the NTSC (United States TV standard) and PAL (one of the European TV standards). The PAL GTIA has been designed so that most programs will run without being modified. However, some differences may be noticeable. There is a hardware register (PAL) which a program can read to determine whether it is PAL or NTSC and adjust accordingly.

PAL (NTSC/PAL register) Addr.=14

Not Used	D3	D2	D1	Not Used

D3	D2	D1	
1	1	1	NTSC (US TV)
0	0	0	PAL (European TV)

This address reads the TV system type.

7.0) TRIGGER INPUTS:

There are four inputs (T0-T3) that have been used as the inputs to sense the trigger buttons of the joystick controller. These inputs are normally read directly by the microprocessor reading TRIG0 through TRIG3. However, if bit 2 of GRACTL is set to a logic high, these inputs are latched whenever they go to a logic zero. These latches are reset (true) when bit 2 of GRACTL is set to a logic zero.

TRIG0 (Trigger 0 input) Addr.=10
TRIG1 (Trigger 1 input) Addr.=11
TRIG2 (Trigger 2 input) Addr.=12
TRIG3 (Trigger 3 input) Addr.=13

Not Used (Zero Forced)	D0

0 = button pressed
1 = button not pressed

These addresses read the trigger inputs.

8.0) SWITCH I/O:

There are four I/O pin (S0 thru S3) that have been used as switch inputs. This port can be read by a single address which puts the data directly on the data bus. When this address is written to, the data going out of the port is inverted from the data on the data bus. The inputs have internal pull-up resistance to VDD. The outputs are open drain. If the I/O port is to be used as inputs, zero should be written to CONSOL register.

CONSOL (Switch port) Addr.=1F

Not Used (zero forced)	D3	D2	D1	D0

D0 = S0, D1 = S1, D2 = S2, and D3 = S3.

9.0) ELECTRICAL PARAMETERS:

9.0) ELECTRICAL PARAMETERS:

9.1) GENERAL:

9.1.1) Storage temperature $-40^{o}C$ to $+90^{o}C$
9.1.2) Ambient operating temperature $0^{o}C$ to $+70^{o}C$
9.1.3) Failure rate less than 0.1% per 1000 hours
9.1.4) Maximum voltage range on any pin with respect to VSS (Pin 3: substrate) without permanent damage to the chip -0.5V to +9.0V

9.2) D.C. AND OPERATING CHARACTERISTICS:

All voltages are referenced to VSS (pin 3).

	MIN.	TYP.	MAX.	UNIT
VDD (PIN 27)	+4.75		+5.25	VOLTS
IDD (PIN 27)			125.0	mA
NORMAL INPUTS:				
$\overline{HLT}$ (PIN 26), $\overline{CS1}$ (PIN 32),R/W (PIN 33), A2-A4 (PIN 40-PIN 38), A0-A1 (PIN 2-PIN 1), AN0-AN2 (PIN 18-PIN 20), Ø2 (PIN 30)				
V_{IH} INPUT HIGH VOLTAGE:	2.0		VDD	VOLTS
V_{IL} INPUT LOW VOLTAGE:	-0.5		+0.8	VOLTS
$I_{LEAKAGE}$ INPUT LEAKAGE: VIN=7.0 VOLTS			10.0	uA
C_{PIN} PIN CAPACITANCE			7.0	pf
DATA BUS I/O: TRI-STATE OUTPUT D0-D3 (PIN 7-PIN 4)				
INPUT:				
V_{IH} INPUT HIGH VOLTAGE:	2.0		VDD	VOLTS
V_{IL} INPUT LOW VOLTAGE:	-0.5		+0.8	VOLTS
$I_{LEAKAGE}$ INPUT LEAKAGE: OUTPUT TRI-STATED VIN=+7.0 VOLTS			10.0	uA
C_{PIN} PIN CAPACITANCE			15.0	pf
OUTPUT:				
V_{OH} OUTPUT HIGH VOLTAGE: I LOAD=-0.1mA	2.4			VOLTS
V_{OL} OUTPUT LOW VOLTAGE: I LOAD=+1.6mA			0.4	VOLTS
C_{LOAD} LOAD CAPACITANCE			130.0	pf

9.2) D.C. OPERATING CHARACTERISTICS (continued):

9.2) D.C. AND OPERATING CHARACTERISTICS: (CONT.)

	MIN.	TYP.	MAX.	UNIT
DATA BUS I/O: OPEN DRAIN OUTPUT				
D4-D7 (PIN 37-PIN 34)				
INPUT:				
V_{IH} INPUT HIGH VOLTAGE:	2.0		VDD	VOLTS
V_{IL} INPUT LOW VOLTAGE:	-0.5		+0.8	VOLTS
$I_{LEAKAGE}$ INPUT LEAKAGE: VIN=7.0 VOLTS PULL-DOWN IS TURNED OFF			10.0	uA
C_{PIN} PIN CAPACITANCE			10.0	pf
OUTPUT:				
V_{OL} OUTPUT LOW VOLTAGE: I LOAD=+1.6mA			0.4	VOLTS
C_{LOAD} LOAD CAPACITANCE			130.0	pf
OUTPUTS: OPEN DRAIN OUTPUT				
COL (PIN 21), L1-L3 (PIN 22-PIN 24)				
L0 (PIN 31)				
V_{OL} OUTPUT LOW VOLTAGE: I LOAD=+1.6mA			0.4	VOLTS
$I_{LEAKAGE}$ INPUT LEAKAGE: VIN=7.0 VOLTS PULL-DOWN IS TURNED OFF			10.0	uA
C_{LOAD} LOAD CAPACITANCE			25.0	pf
INPUT CLOCK :				
OSC (PIN 28)				
V_{IH} INPUT HIGH VOLTAGE:	2.8		VCC	VOLTS
V_{IL} INPUT LOW VOLTAGE:	-0.5		+0.8	VOLTS
$I_{LEAKAGE}$ INPUT LEAKAGE: VIN=7.0 VOLTS			10.0	uA
C_{PIN} PIN CAPACITANCE			7.0	pf
$\overline{\text{CSYNC}}$ OUTPUT:				
$\overline{\text{CSYNC}}$ (PIN 25)				
V_{OH} OUTPUT HIGH VOLTAGE: I LOAD=-100.0 uA	2.8			VOLTS
V_{OL} OUTPUT LOW VOLTAGE: I LOAD=+1.6mA			0.4	VOLTS
C_{LOAD} LOAD CAPACITANCE			25.0	pf

9.2) D.C. & OPERATING CHARACTERISTICS (continued):

9.2) D.C. AND OPERATING CHARACTERISTICS: (CONT.)

	MIN.	TYP.	MAX.	UNIT
FAST PHASE CLOCK OUTPUT: (FOR ANTIC)				
FØ0 (PIN 29)				
V_{OH} OUTPUT HIGH VOLTAGE: I LOAD=-100.0 uA	2.8			VOLTS
V_{OL} OUTPUT LOW VOLTAGE: I LOAD=+1.6mA			0.4	VOLTS
C_{LOAD} LOAD CAPACITANCE			25.0	pf
SWITCH BUS I/O: OPEN DRAIN OUTPUT				
S0-S3 (PIN 12-PIN 15)				
INPUT: (WITH INTERNAL PULL UP DEVICE)				
V_{IH} INPUT HIGH VOLTAGE:	2.0		VDD	VOLTS
V_{IL} INPUT LOW VOLTAGE:	-0.5		+0.8	VOLTS
$I_{PULL-UP}$ INPUT PULL-UP CURRENT:VIN= 2.4V.	100.0			uA
C_{PIN} PIN CAPACITANCE			25.0	pf
OUTPUT:				
V_{OL} OUTPUT LOW VOLTAGE: I LOAD=+1.6mA			0.4	VOLTS
C_{LOAD} LOAD CAPACITANCE			30.0	pf
TRIGGER INPUTS:(WITH INTERNAL PULL-UP DEVICE				
T0-T3 (PIN 8-PIN 11)				
V_{IH} INPUT HIGH VOLTAGE:	2.0		VDD	VOLTS
V_{IL} INPUT LOW VOLTAGE:	-0.5		+0.8	VOLTS
$I_{PULL-UP}$ INPUT PULL-UP CURRENT:VIN= 2.4V.	100.0			uA
C_{PIN} PIN CAPACITANCE			25.0	pf
DEL INPUT: COLOR DELAY LINE ADJUSTMENT				
DEL (PIN 17)				
V_{ADJUST} INPUT ADJUSTMENT VOLTAGE:	3.0		8.0	VOLTS
$I_{LEAKAGE}$ INPUT LEAKAGE: VIN=7.0 VOLTS			10.0	uA
C_{PIN} PIN CAPACITANCE			50.0	pf

9.3) DYNAMIC OPERATING CHARACTERISTICS:

(VDD = 5V±5% TA = 0° to 70°C)

Parameter	Note	Signal Type	Symbol	MIN.	MAX.	UNIT
CLOCK TIMING:						
Ø2 INPUT:						
LOGIC HIGH TIME			T_{HI}	230	260	nS
RISE TIME			T_R		25	nS
FALL TIME			T_F		25	nS
OSC INPUT:						
LOGIC HIGH TIME			T_{HI}	135	145	nS
RISE TIME			T_R		15	nS
FALL TIME			T_F		15	nS
FAST PHASE CLOCK OUTPUT: FØ0						
LOGIC HIGH TIME			T_{HI}	105	135	nS
RISE TIME			T_R		30	nS
FALL TIME			T_F		25	nS
OUTPUT DELAY TIME	1	ALE OSC	T_{DS}		130	nS
INPUT TIMING:						
R/W SETUP TIME		BLE Ø2	T_{RWS}	130		nS
R/W HOLD TIME		ATE Ø2	T_{RWH}	30		nS
ADDRESS SETUP TIME		BLE Ø2	T_{ADS}	130		nS
ADDRESS HOLD TIME		ALE Ø2	T_{ADH}	30		nS
CHIP SELECT SETUP TIME		BLE Ø2	T_{CSS}	50		nS
CHIP SELECT HOLD TIME		ATE Ø2	T_{CSH}	30		nS
DATA SETUP TIME : D0-D7		BTE Ø2	T_{DSH}	50		nS
DATA HOLD TIME : D0-D7		ATE Ø2	T_{DHW}	10		nS
DATA SETUP TIME :T0-T3,S0-S3		BLE Ø2	T_{DS}	100		nS
DATA HOLD TIME :T0-T3,S0-S3		ATE Ø2	T_{DH}	100		nS
DATA SETUP TIME : AN0-AN2		BLE OSC	T_{DS}	50		nS
DATA HOLD TIME : AN0-AN2		ALE OSC	T_{DH}	130		nS
DATA SETUP TIME : $\overline{HALT}$		BTE Ø2	T_{DS}	50		nS
DATA HOLD TIME : $\overline{HALT}$		ATE Ø2	T_{DH}	50		nS

NOTE:
1) OUTPUT LOAD AT 25pF + 1 TTL LOAD.

9.3) DYNAMIC OPERATING CHARACTERISTICS (continued):

9.3) DYNAMIC OPERATING CHARACTERISTICS: (CONT.)

(VDD = 5V±5% TA = 0° to 70°C)

Parameter	Note	Signal Type	Symbol	MIN.	MAX.	UNIT
OUTPUT TIMING:						
DATA SETUP TIME : D0-D7	3	BTE Ø2	T_{DSR}		50	nS
DATA HOLD TIME : D0-D7	3	ATE Ø2	T_{DHR}	20		nS
DATA SETUP TIME : $\overline{CSYNC}$	1	ATE OSC	T_{DS}		400	nS
DATA HOLD TIME : $\overline{CSYNC}$	1	ATE OSC	T_{DH}	40		nS
DATA SETUP TIME : L0-L3	1	ALE OSC	T_{DS}		450	nS
DATA HOLD TIME : L0-L3	1	ALE OSC	T_{DH}	45		nS
DATA SETUP TIME : S0-S3	2	ATE Ø2	T_{DS}		800	nS
DATA HOLD TIME : S0-S3	2	ATE Ø2	T_{DH}	80		nS
COLOR DELAY LINE OUTPUT: NOTE: Output is OPEN DRAIN and pull up effects leading edge delay.						
OUTPUT DELAY TIME: WITH V_{DEL} (PIN 17)=7.0V and WITH COLOR= C3 C2 C1 C0	1	ATE OSC	T_{DD}			
NO COLOR OUT 0 0 0 0						
0 0 0 1					167	nS
0 0 1 0					188	nS
0 0 1 1					209	nS
0 1 0 0					230	nS
0 1 0 1					251	nS
0 1 1 0					272	nS
0 1 1 1					293	nS
1 0 0 0					314	nS
1 0 0 1					335	nS
1 0 1 0					356	nS
1 0 1 1					377	nS
1 1 0 0					398	nS
1 1 0 1					419	nS
1 1 1 0					440	nS
1 1 1 1					461	nS

NOTES:

1) OUTPUT LOAD AT 25pF + 1 TTL
2) OUTPUT LOAD AT 30pF + 1 TTL
3) OUTPUT LOAD AT 130pF + 1 TTL

9.3) DYNAMIC OPERATING CHARACTERISTICS (continued):

9.3) DYNAMIC OPERATING CHARACTERISTICS: (CONT.)

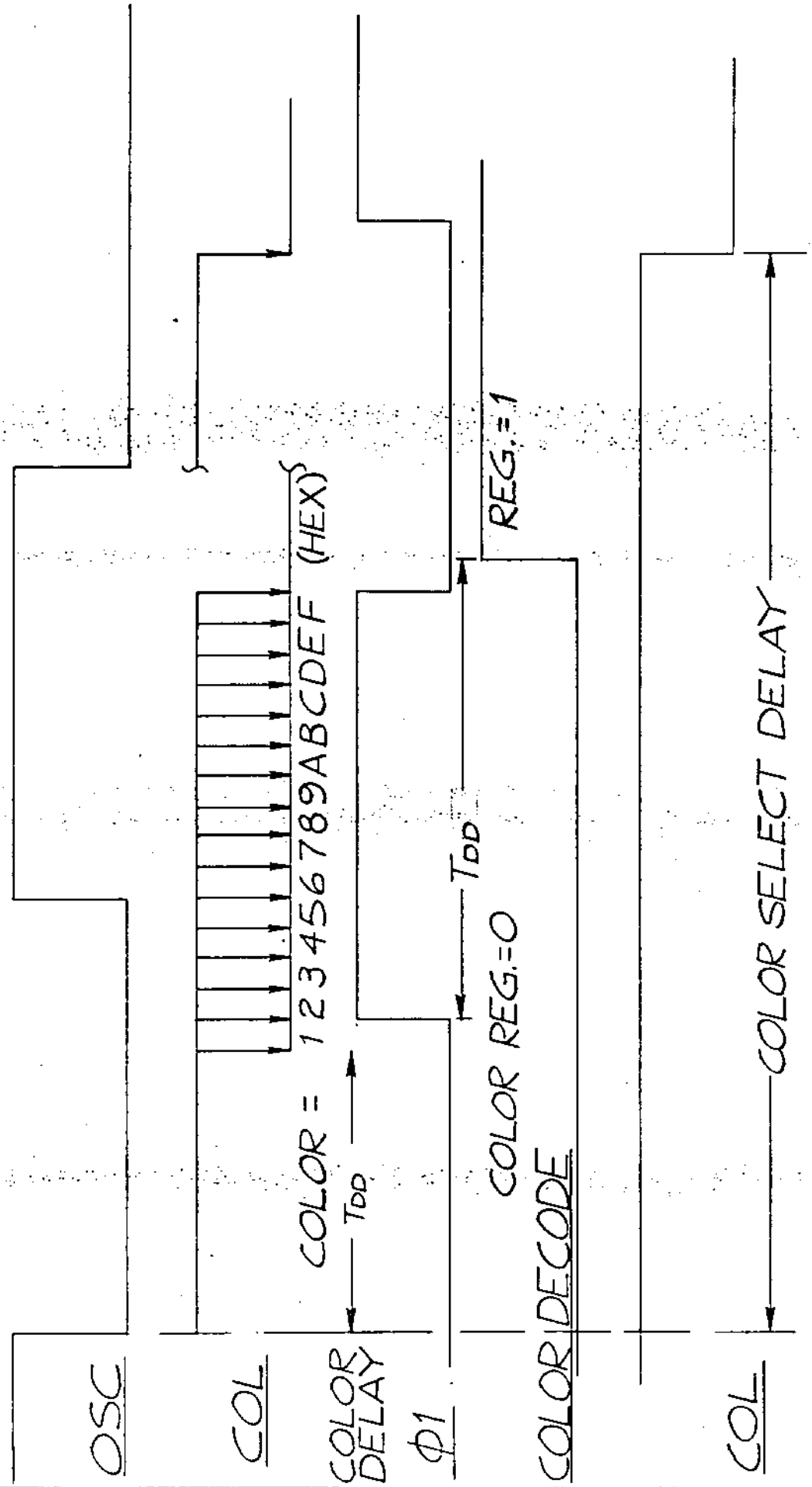
(VDD = 5V±5% TA = 0° to 70°C)

Parameter	Note	Signal Type	Symbol	MIN.	MAX.	UNIT
OUTPUT TIMING: (CONT.)						
COLOR DELAY LINE OUTPUT: (CONT.)						
OUTPUT DELAY TIME: WITH V_{DEL} (PIN 17)=5.0V and	1	ATE OSC	T_{DD}			
WITH COLOR= C3 C2 C1 C0						
NO COLOR OUT 0 0 0 0						
0 0 0 1					190	nS
0 0 1 0					225	nS
0 0 1 1					260	nS
0 1 0 0					295	nS
0 1 0 1					330	nS
0 1 1 0					365	nS
0 1 1 1					400	nS
1 0 0 0					435	nS
1 0 0 1					470	nS
1 0 1 0					505	nS
1 0 1 1					540	nS
1 1 0 0					575	nS
1 1 0 1					610	nS
1 1 1 0					645	nS
1 1 1 1					680	nS
COLOR SELECT DELAY: Changing from a color reg.= HEX 0 to another reg.= HEX 1 and V_{DEL} (PIN 17)=5.0 Volts	1	ATE OSC	T_{DD}		610	nS

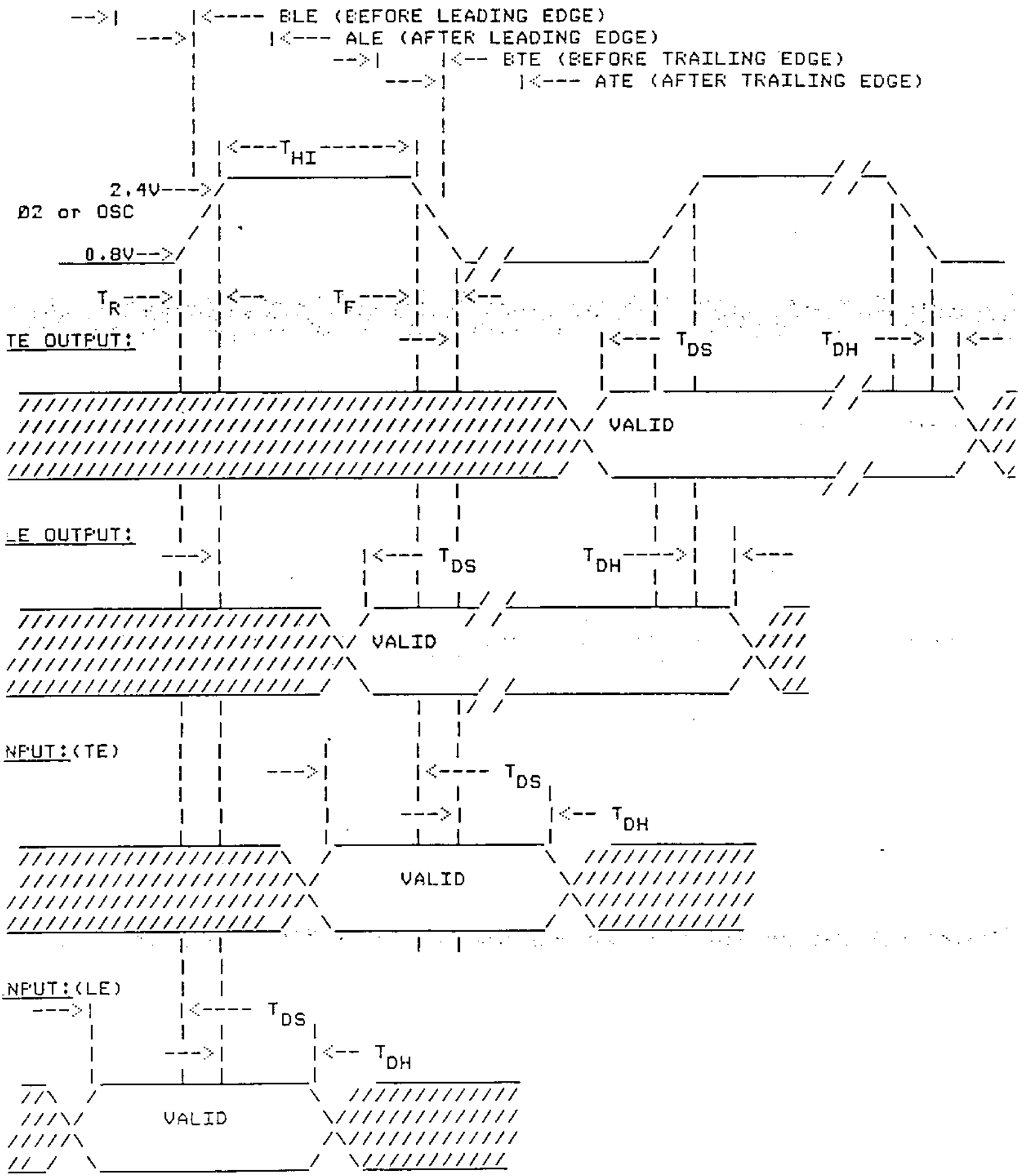
NOTES:

1) OUTPUT LOAD AT 25pF + 1 TTL

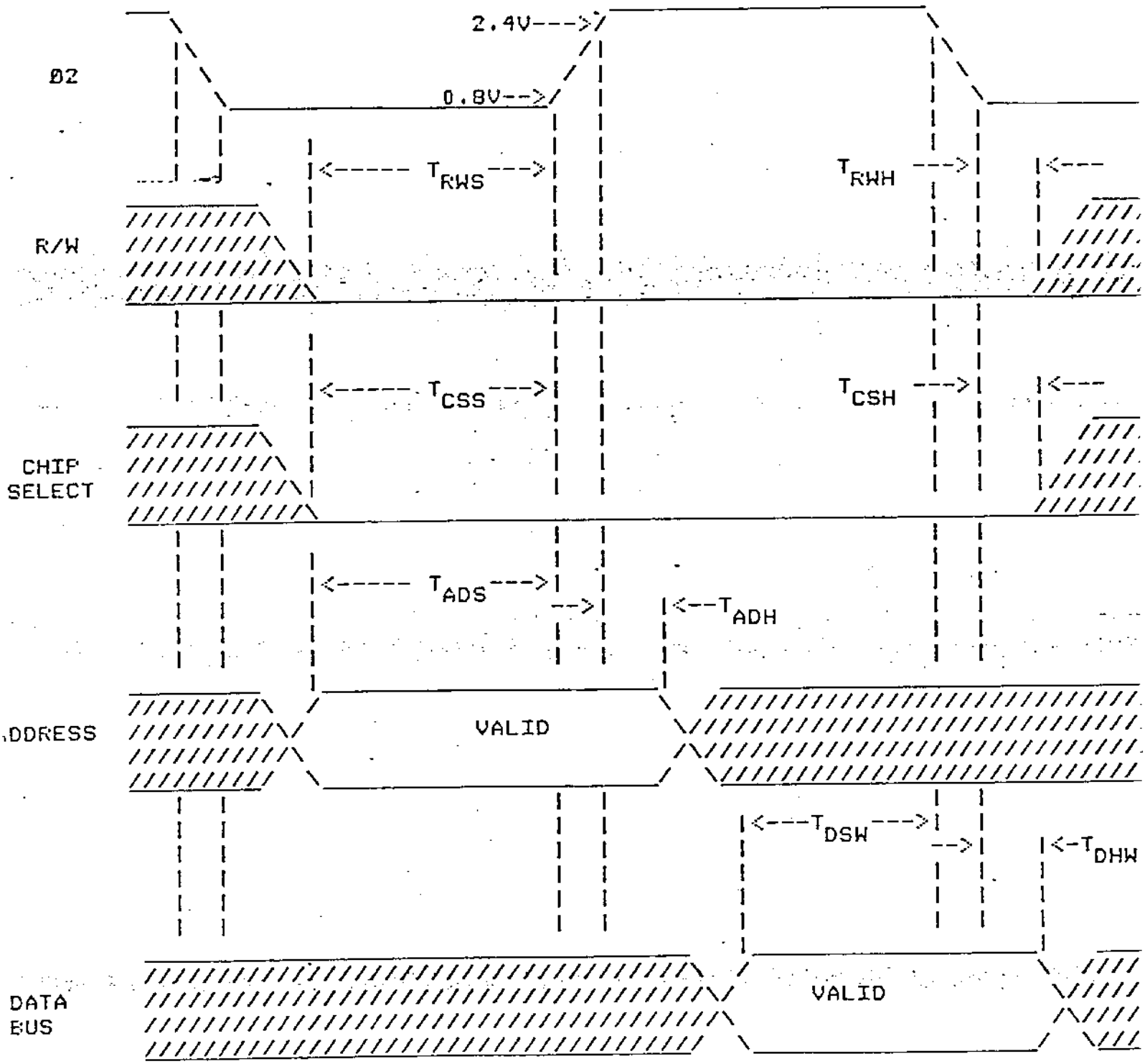
9.3) DYNAMIC OPERATING CHARACTERISTICS (Continued):



.4) I/O TIMING:


BLE (BEFORE LEADING EDGE)
ALE (AFTER LEADING EDGE)
BTE (BEFORE TRAILING EDGE)
ATE (AFTER TRAILING EDGE)
T_{HI}
2.4V
Ø2 or OSC
0.8V
T_R
T_F
TE OUTPUT:
T_{DS}
T_{DH}
VALID
LE OUTPUT:
NPUT:(TE)
NPUT:(LE)

.5) WRITE I/O TIMING: (MICROPROCESSOR WRITING TO THE GTIA)



NOTE: ADDRESSES ARE CLOCKED IN ON THE LEADING EDGE OF Ø2.

GTIA PIN LIST

PIN #	PIN NAME	DESCRIPTION
1	A1	Address Input
2	A0	Address Input
3	VSS	Ground
4	D3	Data Bus I/O
5	D2	Data Bus I/O
6	D1	Data Bus I/O
7	D0	Data Bus I/O
8	T0	Trigger Input with internal pull-up
9	T1	Trigger Input with internal pull-up
10	T2	Trigger Input with internal pull-up
11	T3	Trigger Input with internal pull-up
12	S0	Switch Data I/O
13	S1	Switch Data I/O
14	S2	Switch Data I/O
15	S3	Switch Data I/O
16	N/C	NOT CONNECTED
17	DEL	Color delay line adjustment Input
18	AN0	ANTIC interface Input
19	AN1	ANTIC interface Input
20	AN2	ANTIC interface Input
21	COL	Color frequency Output
22	L1	Luminance Output
23	L2	Luminance Output
24	L3	Luminance Output
25	CSYNC	Composite Sync Output
26	$\overline{\text{HALT}}$	Halt Output
27	VDD	Power
28	OSC	Oscillator Input
29	FØ0	Fast phase clock Output
30	Ø2	Computer phase 2 Input
31	L0	Luminance Output
32	CS1	Chip Select Input
33	R/W	Read/Write Input
34	D7	Data Bus I/O
35	D6	Data Bus I/O
36	D5	Data Bus I/O
37	D4	Data Bus I/O
38	A4	Address Input
39	A3	Address Input
40	A2	Address Input

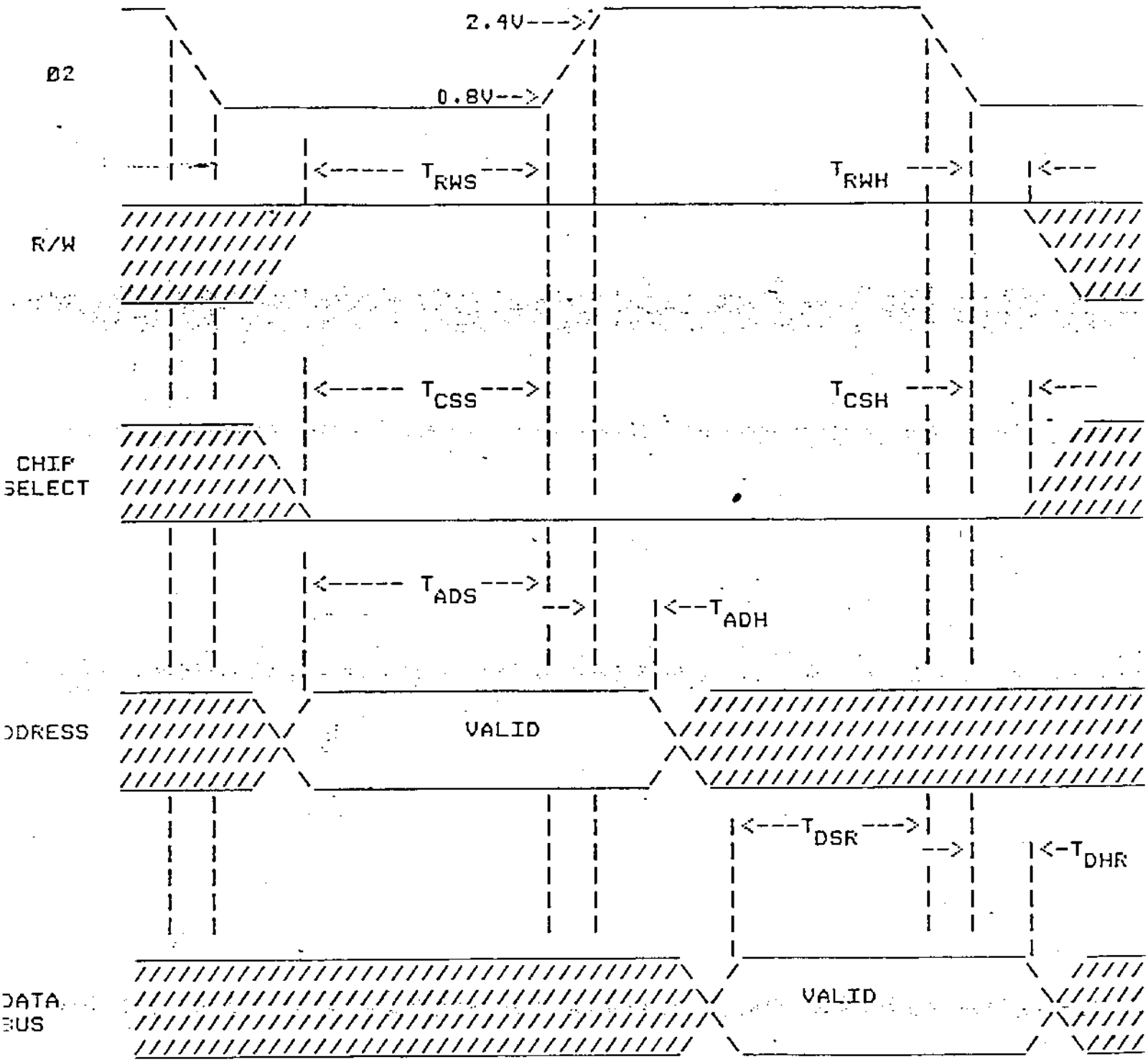
ATARI

TITLE GTIA CHIP (NTSC)

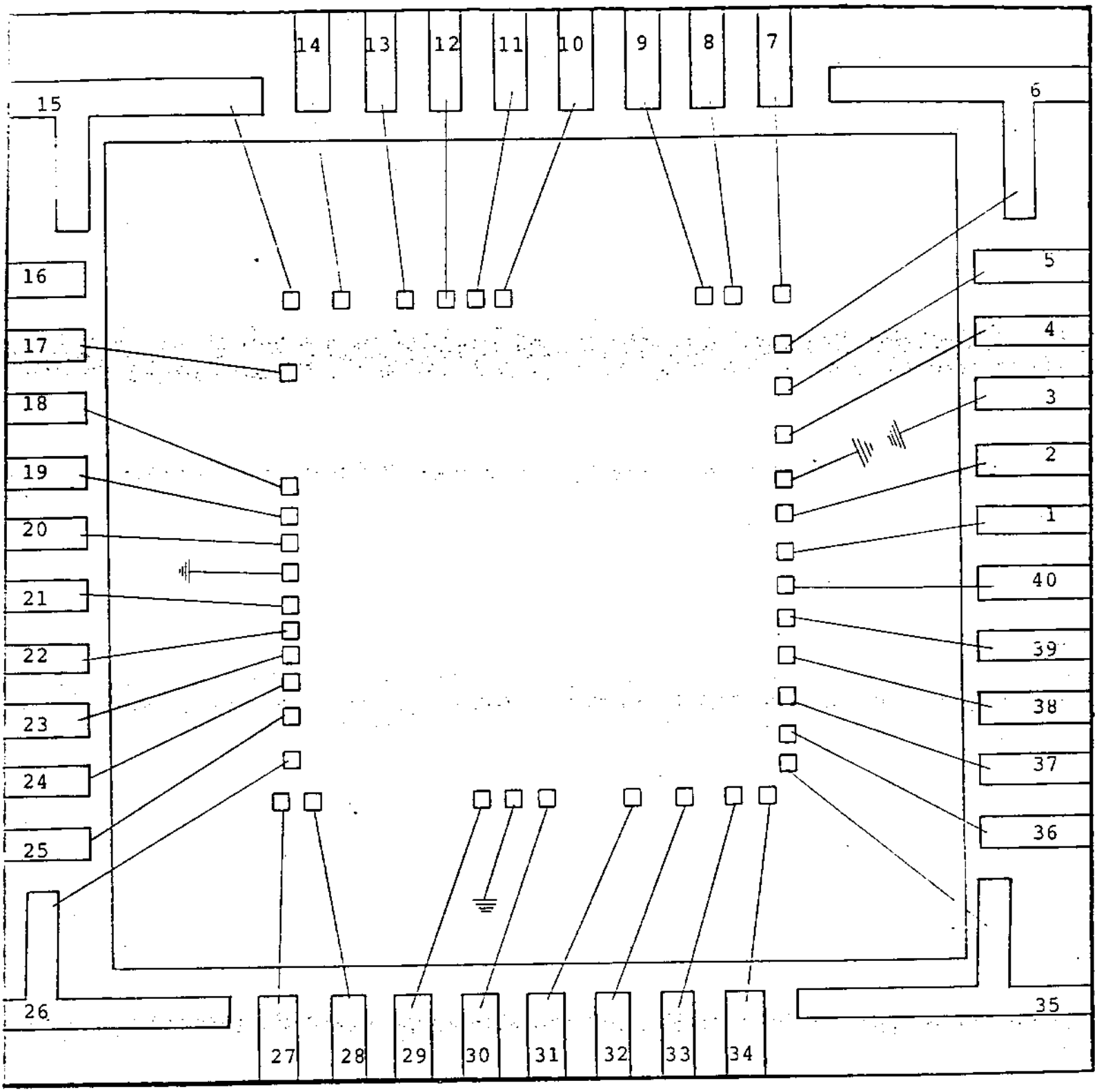
GTIA ADDRESS TABLE

	WRITE		READ	
ddress	Name	Description	Name	Description
0	HPOSP0	Horz. Posit. Player 0	M0PF	Read Missile To
1	HPOSP1	Horz. Posit. Player 1	M1PF	Playfield Collision
2	HPOSP2	Horz. Posit. Player 2	M2PF	
3	HPOSP3	Horz. Posit. Player 3	M3PF	
4	HPOSM0	Horz. Posit. Missile 0	P0PF	Read Player To
5	HPOSM1	Horz. Posit. Missile 1	P1PF	Playfield Collision
6	HPOSM2	Horz. Posit. Missile 2	P2PF	
7	HPOSM3	Horz. Posit. Missile 3	P3PF	
8	SIZEP0	Size Player 0	M0PL	Read Missile To
9	SIZEP1	Size Player 1	M1PL	Player Collisions
A	SIZEP2	Size Player 2	M2PL	
B	SIZEP3	Size Player 3	M3PL	
C	SIZEM	Size All Missiles	P0PL	Read Player To
D	GRAFP0	Graphics Player 0	P1PL	Player Collisions
E	GRAFP1	Graphics Player 1	P2PL	
F	GRAFP2	Graphics Player 2	P3PL	
10	GRAFP3	Graphics Player 3	TRIG0	Read Joystick
11	GRAFM	Graphics All Missiles	TRIG1	Trigger Buttons
12	COLPM0	Color-lum of Player-Missile 0	TRIG2	
13	COLPM1	Color-lum of Player-Missile 1	TRIG3	
14	COLPM2	Color-lum of Player-Missile 2	PAL	Read PAL/NTSC Bits
15	COLPM3	Color-lum of Player-Missile 3		
16	COLPF0	Color-lum of Playfield 0		
17	COLPF1	Color-lum of Playfield 1		
18	COLPF2	Color-lum of Playfield 2		
19	COLPF3	Color-lum of Playfield 3		
1A	COLBK	Color-lum of Background		
1B	PRIOR	Priority Select		
1C	VDELAY	Vertical Delay		
1D	GRACTL	Graphic Control		
1E	HITCLR	Collision Clear		
1F	CONSOL	Write to Switch I/O Port	CONSOL	Read from Switch I/O Port

(6) READ I/O TIMING: (MICROPROCESSOR READING FROM THE GTIA)



NOTE: ADDRESSES ARE CLOCKED IN ON THE LEADING EDGE OF Ø2.



SCALE 20:1

6 MICRON DESIGN RULE

DIE SIZE : 163 MILS X 174 MILS

GTIA BONDING DIAGRAM (NTSC VERSION)

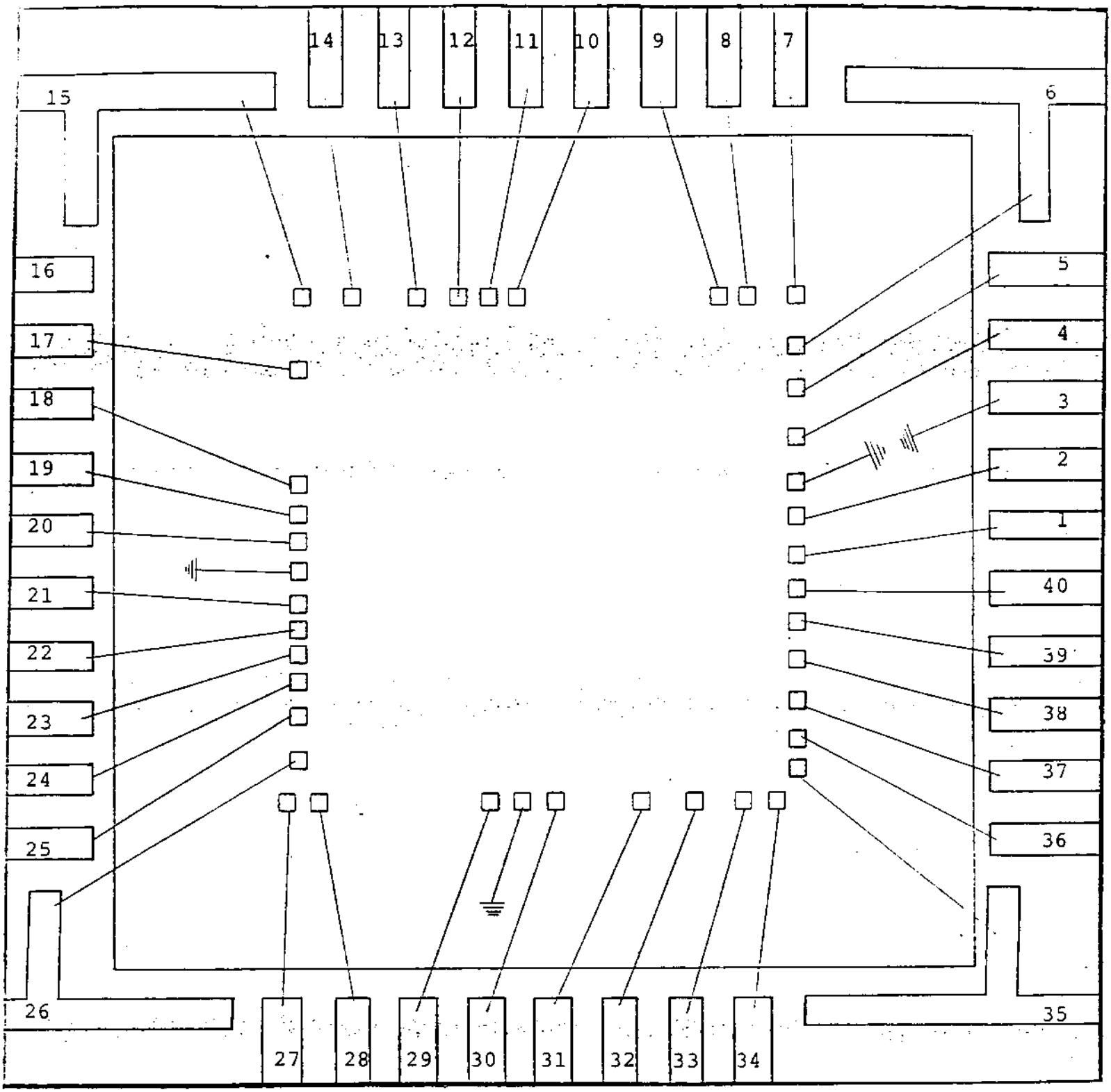
ATARI®	TITLE	GTIA CHIP (NTSC)

GTIA PIN LIST

PIN #	PIN NAME	DESCRIPTION
1	A1	Address Input
2	A0	Address Input
3	VSS	Ground
4	D3	Data Bus I/O
5	D2	Data Bus I/O
6	D1	Data Bus I/O
7	D0	Data Bus I/O
8	T0	Trigger Input with internal pull-up
9	T1	Trigger Input with internal pull-up
10	T2	Trigger Input with internal pull-up
11	T3	Trigger Input with internal pull-up
12	S0	Switch Data I/O
13	S1	Switch Data I/O
14	S2	Switch Data I/O
15	S3	Switch Data I/O
16	N/C	NOT CONNECTED
17	DEL	Color delay line adjustment Input
18	AN0	ANTIC interface Input
19	AN1	ANTIC interface Input
20	AN2	ANTIC interface Input
21	COL	Color frequency Output
22	L1	Luminance Output
23	L2	Luminance Output
24	L3	Luminance Output
25	CSYNC	Composite Sync Output
26	$\overline{\text{HALT}}$	Halt Output
27	VDD	Power
28	OSC	Oscillator Input
29	FØ0	Fast phase clock Output
30	Ø2	Computer phase 2 Input
31	L0	Luminance Output
32	CS1	Chip Select Input
33	R/W	Read/Write Input
34	D7	Data Bus I/O
35	D6	Data Bus I/O
36	D5	Data Bus I/O
37	D4	Data Bus I/O
38	A4	Address Input
39	A3	Address Input
40	A2	Address Input

ATARI

TITLE GTIA CHIP (NTSC)



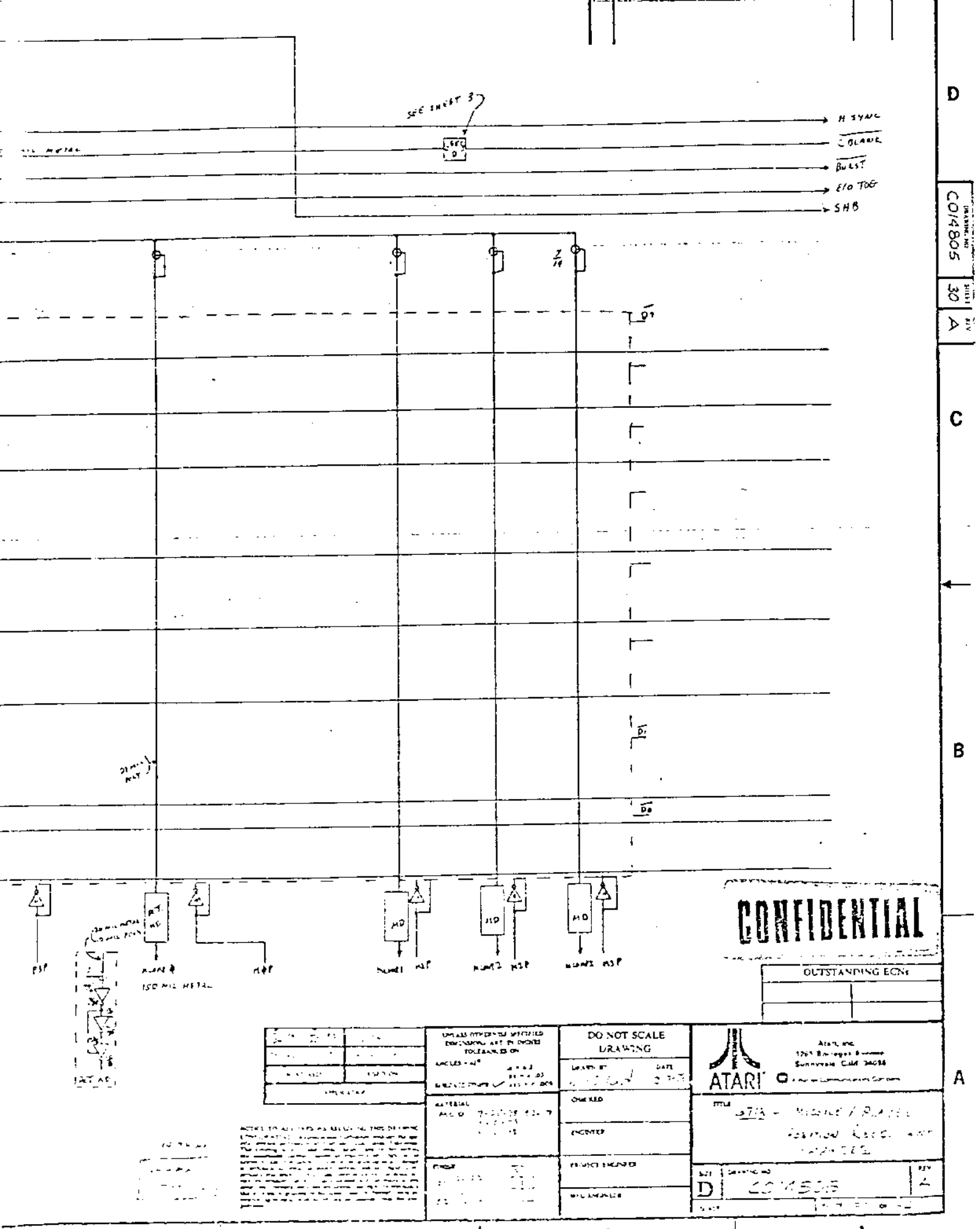
SCALE 20:1

6 MICRON DESIGN RULE

DIE SIZE : 163 MILS X 174 MILS

GTIA BONDING DIAGRAM (NTSC VERSION)

ATARI®	TITLE	GTIA CHIP (NTSC)



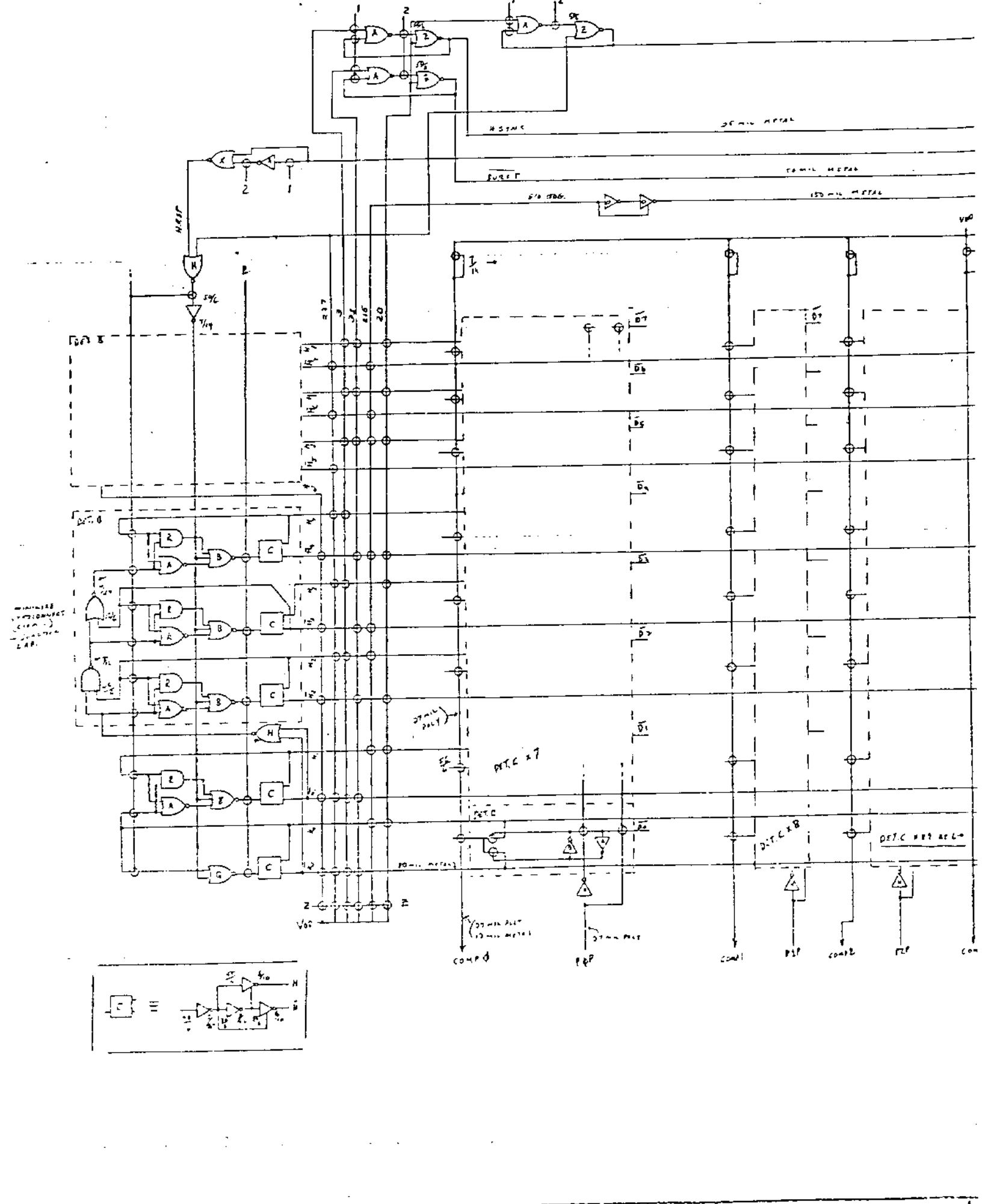
OUTSTANDING ECNs

DO NOT SCALE DRAWING

ATARI

SIZE	DRAWING NO	REV
D	C014805	A

DRAWING NO	SHEET	REV
C014805	30	A



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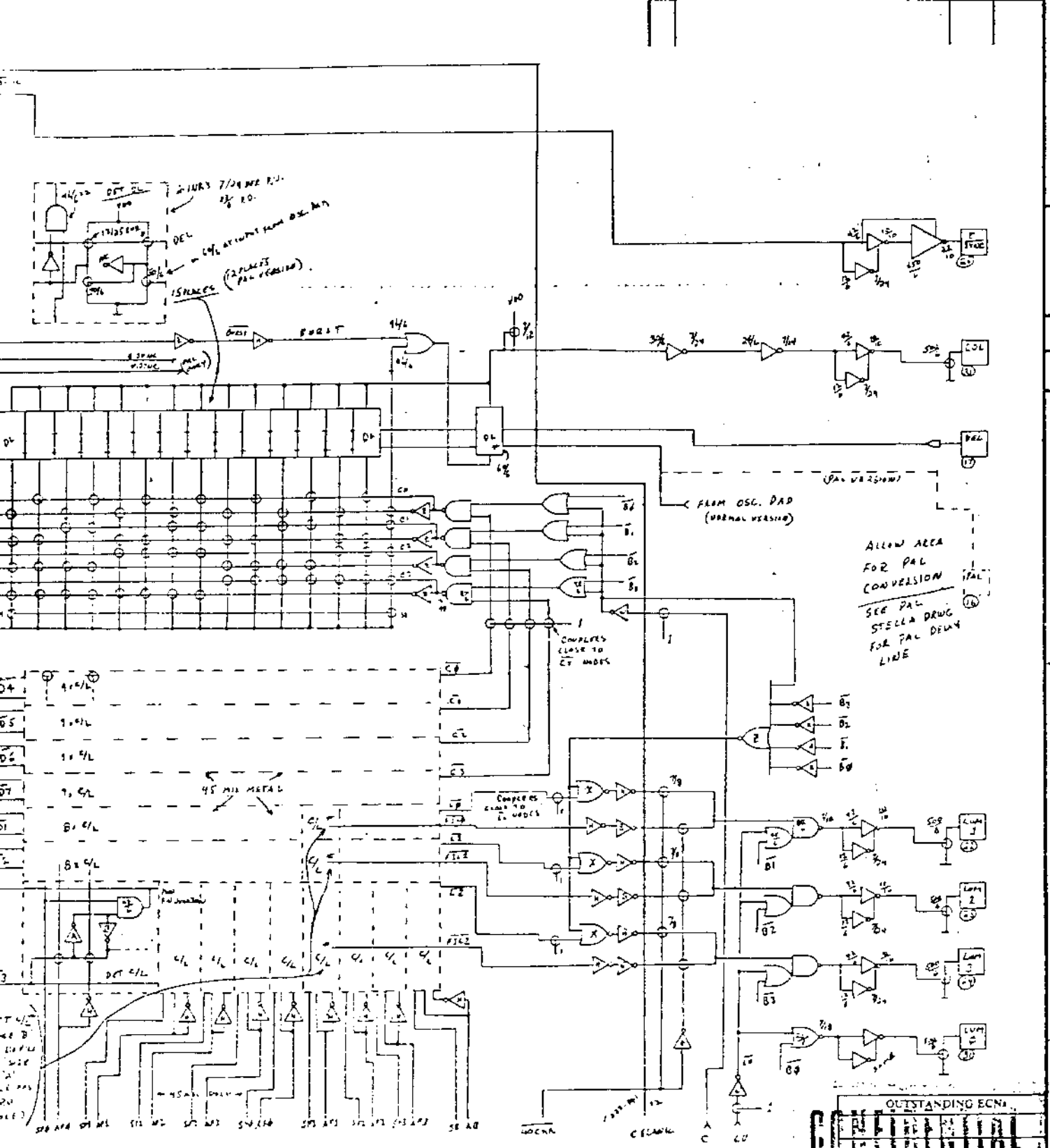
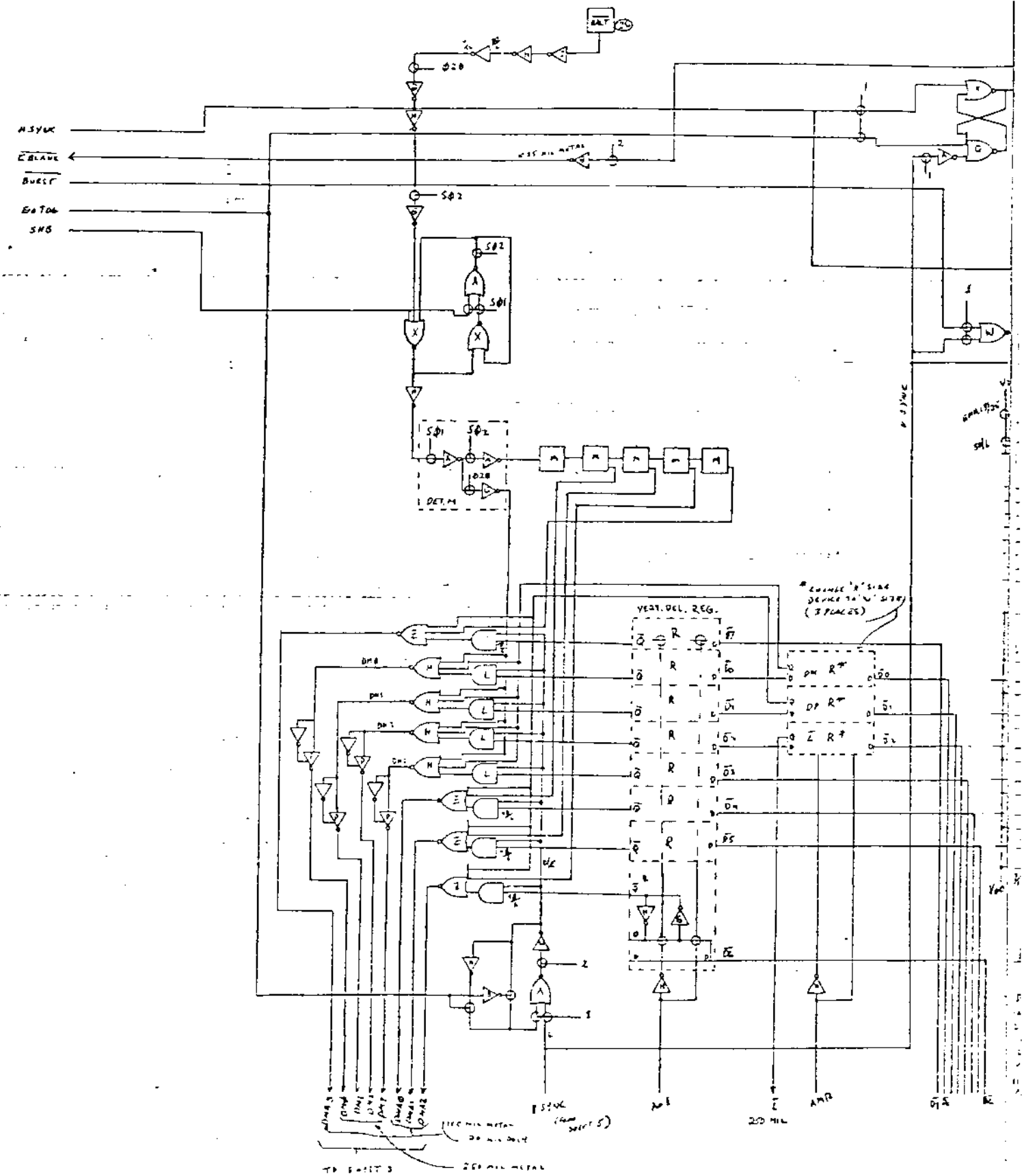
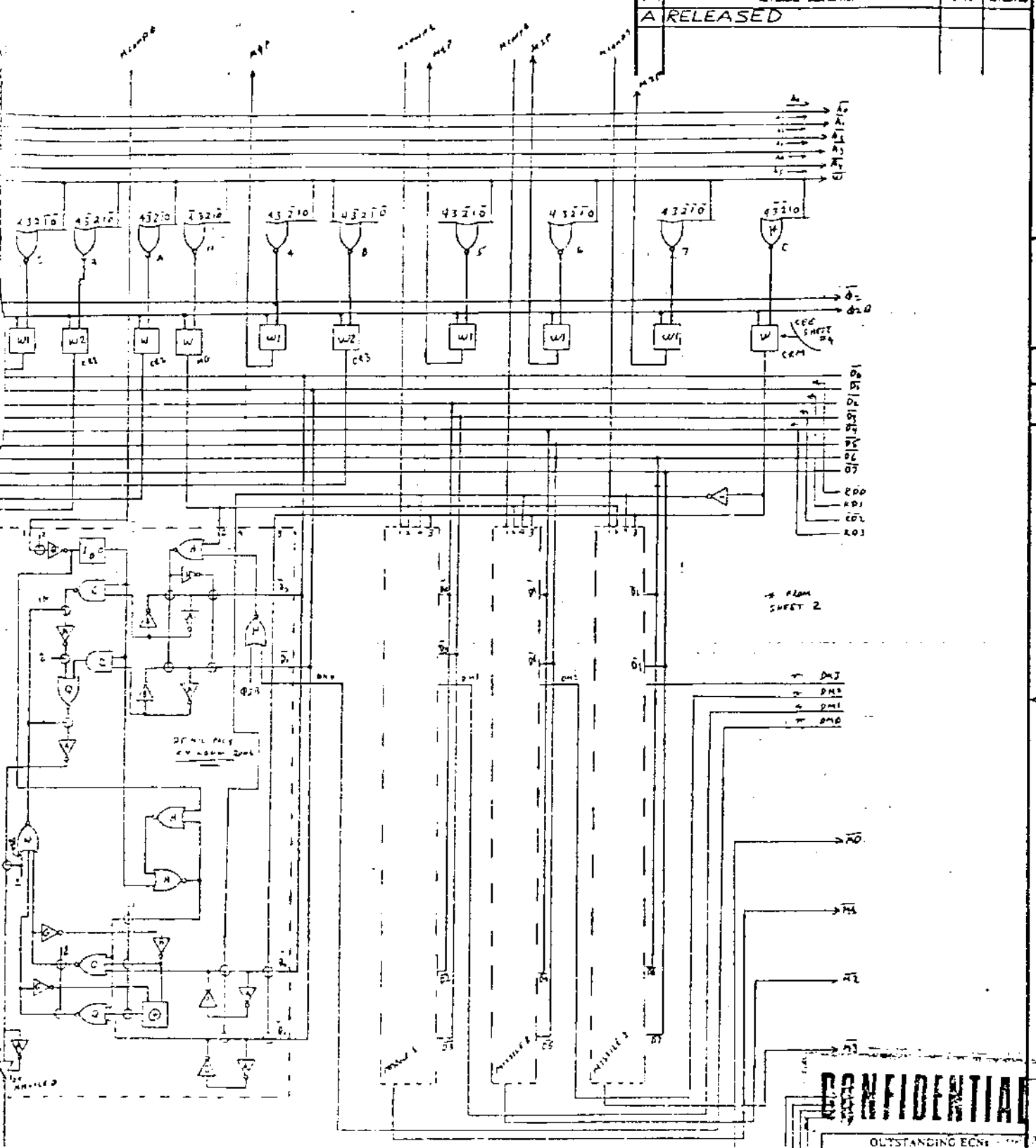
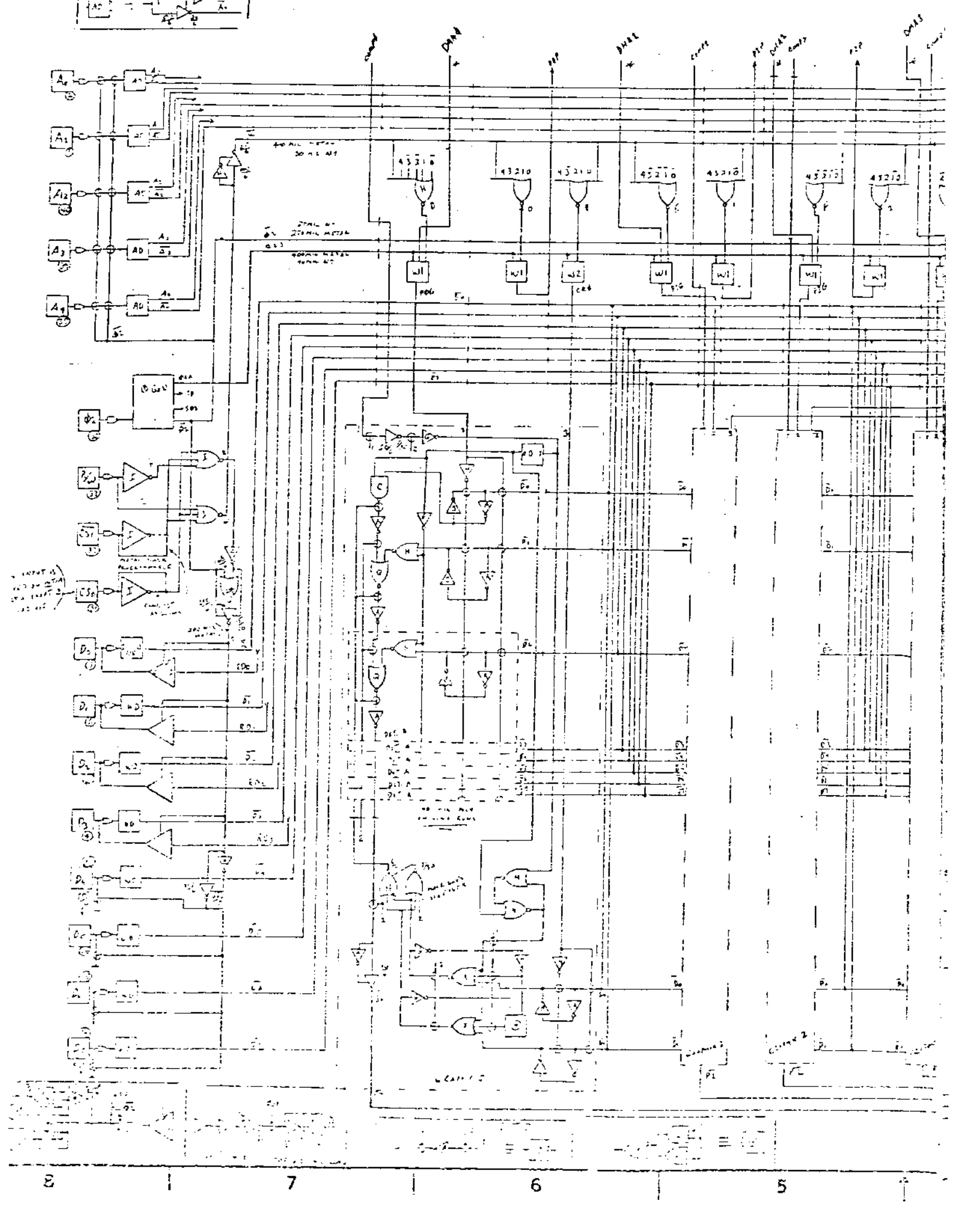
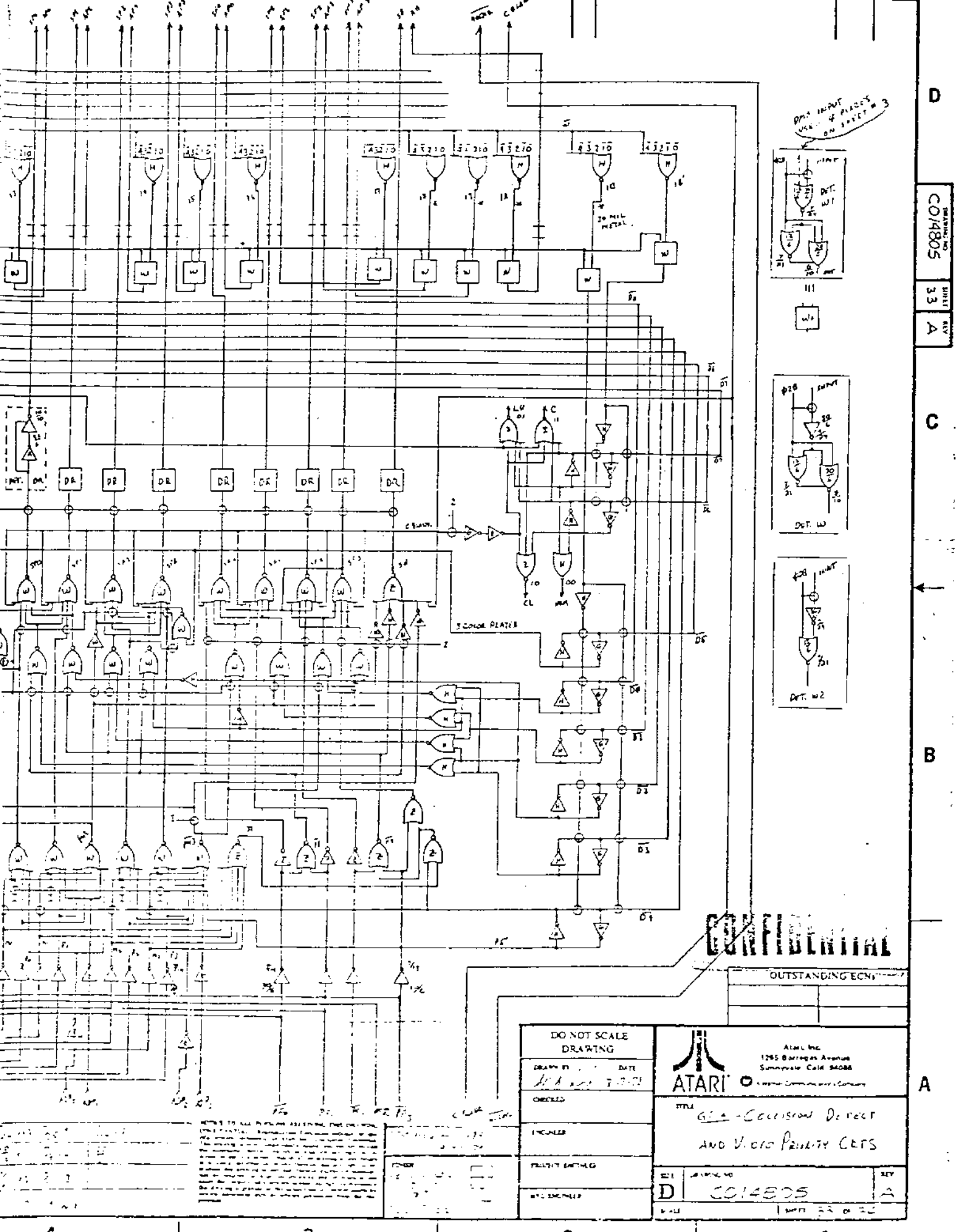

FROM OSC. PAD
(NORMAL VERSION)
(PAL VERSION)
ALLOW AREA FOR PAL CONVERSION
SEE PAL STELLA DRWG FOR PAL DELAY LINE
45 MIL METAL
OUTSTANDING ECNs
CONFIDENTIAL
DO NOT SCALE DRAWING
ATARI
D
C014805
A

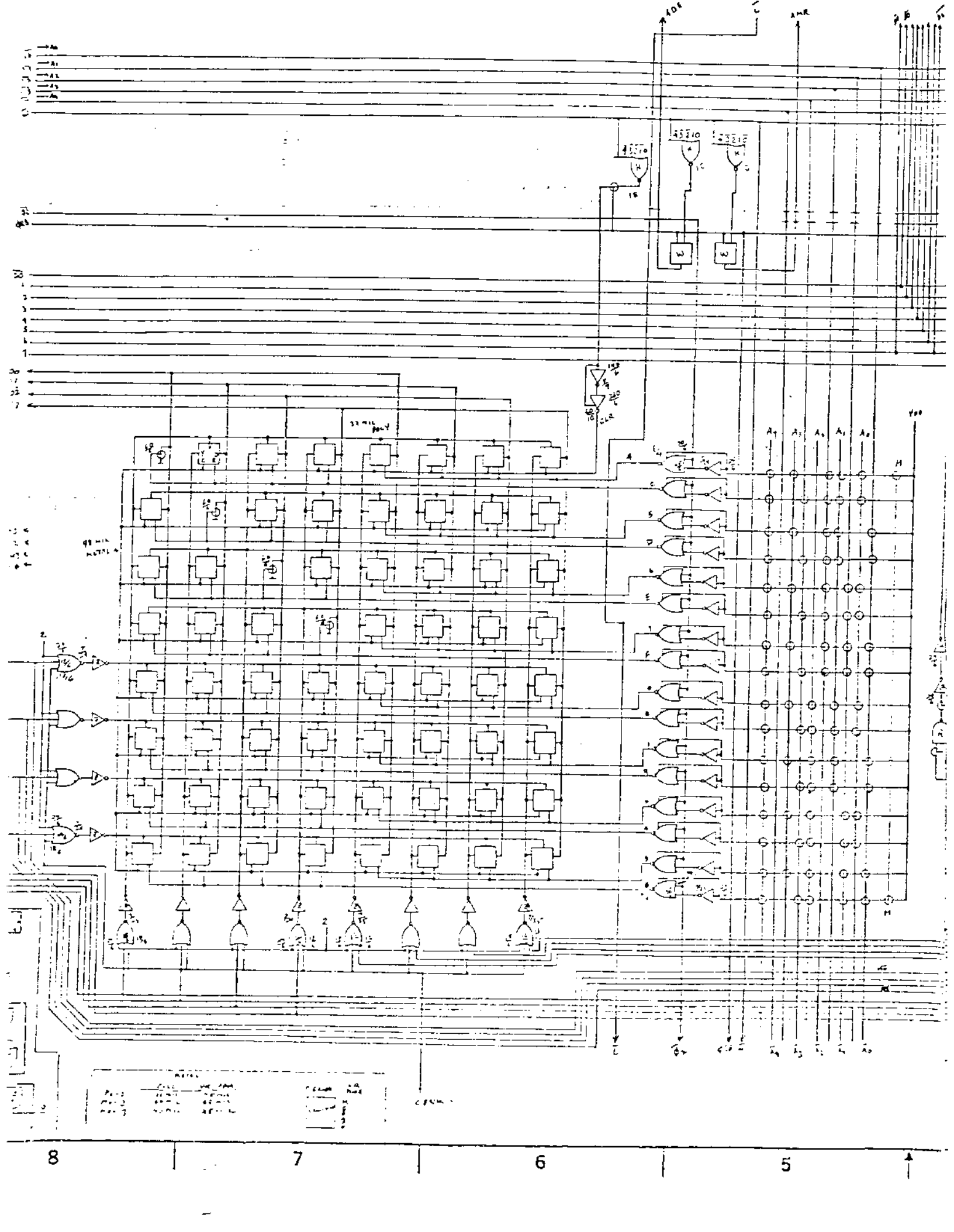

MSYNC
CSLAVE
BUSCT
EXTOG
SMS
SΦ2
SΦ1
DET. M
VERT. DEL. REG.
DM R*
DP R*
Z R*
DM8
DM7
DM6
DM5
DM4
DM3
DM2
DM1
DM0
Z SYNC
(FROM SHEET 5)
TO SHEET 3
250 MIL


A RELEASED
CONFIDENTIAL
OUTSTANDING ECNs
DO NOT SCALE DRAWING
ATARI
CTIA - ADDRESS-DATA DECODES-
PLAYER-MISSILE GRAPHICS
D
C014805
A
DRAWING NO. C014805
SHEET 32
REV A
4
3
2
1



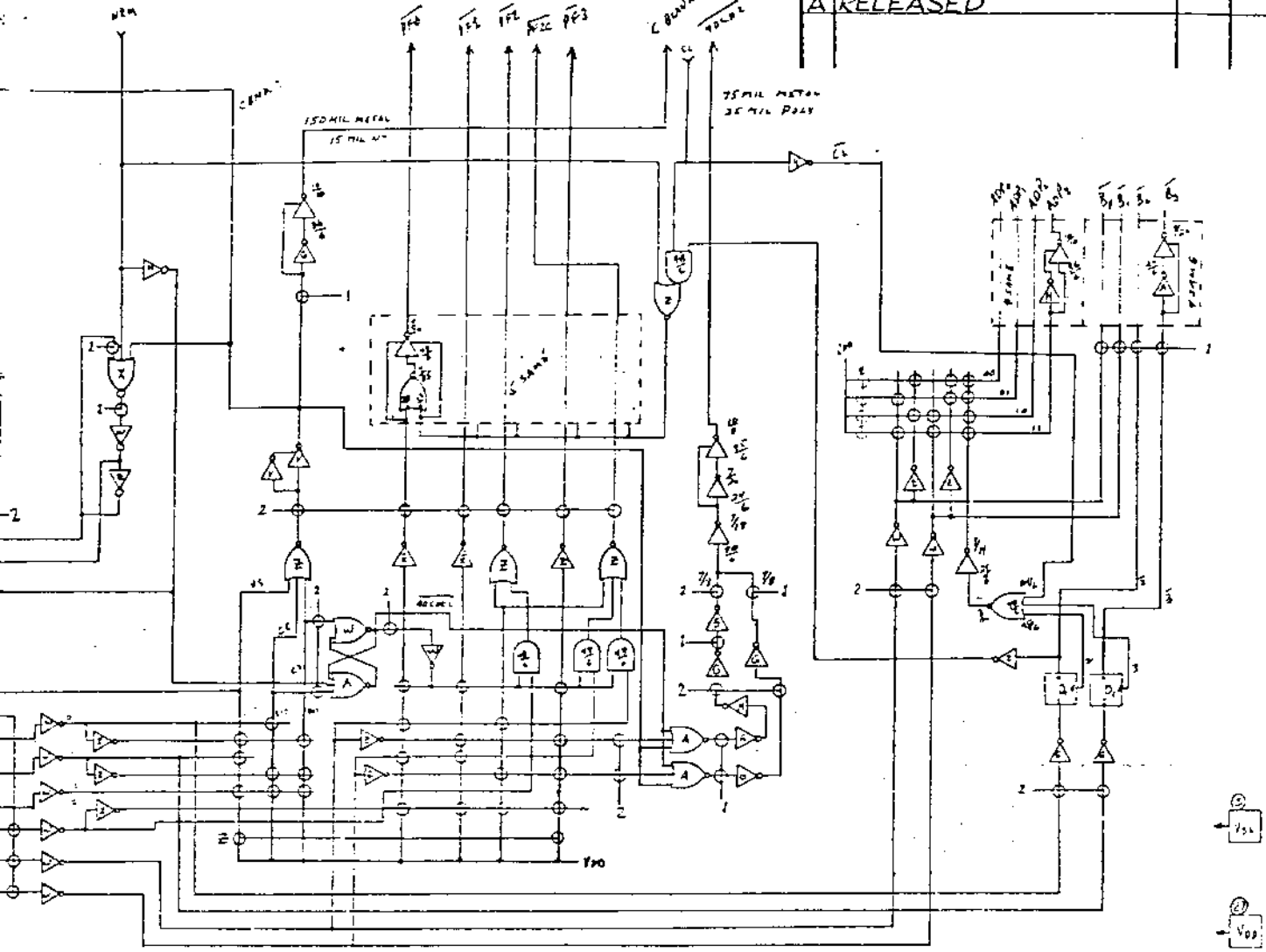
8 | 7 | 6 | 5

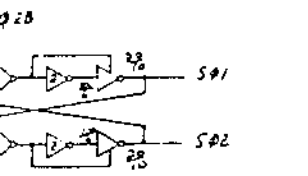

CONFIDENTIAL
OUTSTANDING ECN
DO NOT SCALE DRAWING
ATARI
Atari Inc.
1265 Borregas Avenue
Sunnyvale Calif. 94086
TITLE
G1A - Collision Detect and Video Priority CCTS
SIZE D
DRAWING NO C014805
REV A
SHEET 33 OF 33
DRAWING NO C014805
SHEET 33
REV A
D
C
B
A
4
3
2
1

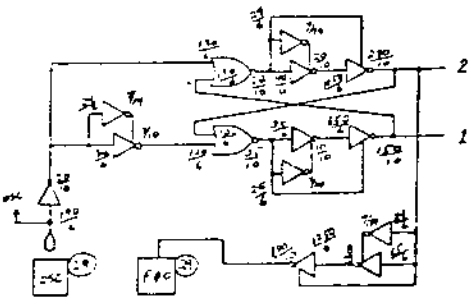


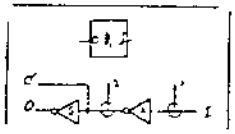
8 7 6 5

RELEASED









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OUTSTANDING ECNs

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ATARI

Atari, Inc.
1265 Borregas Avenue
Sunnyvale Calif 94086

TITLE: STIA - ARITHMETIC INTERFACE AND SWITCH INPUTS

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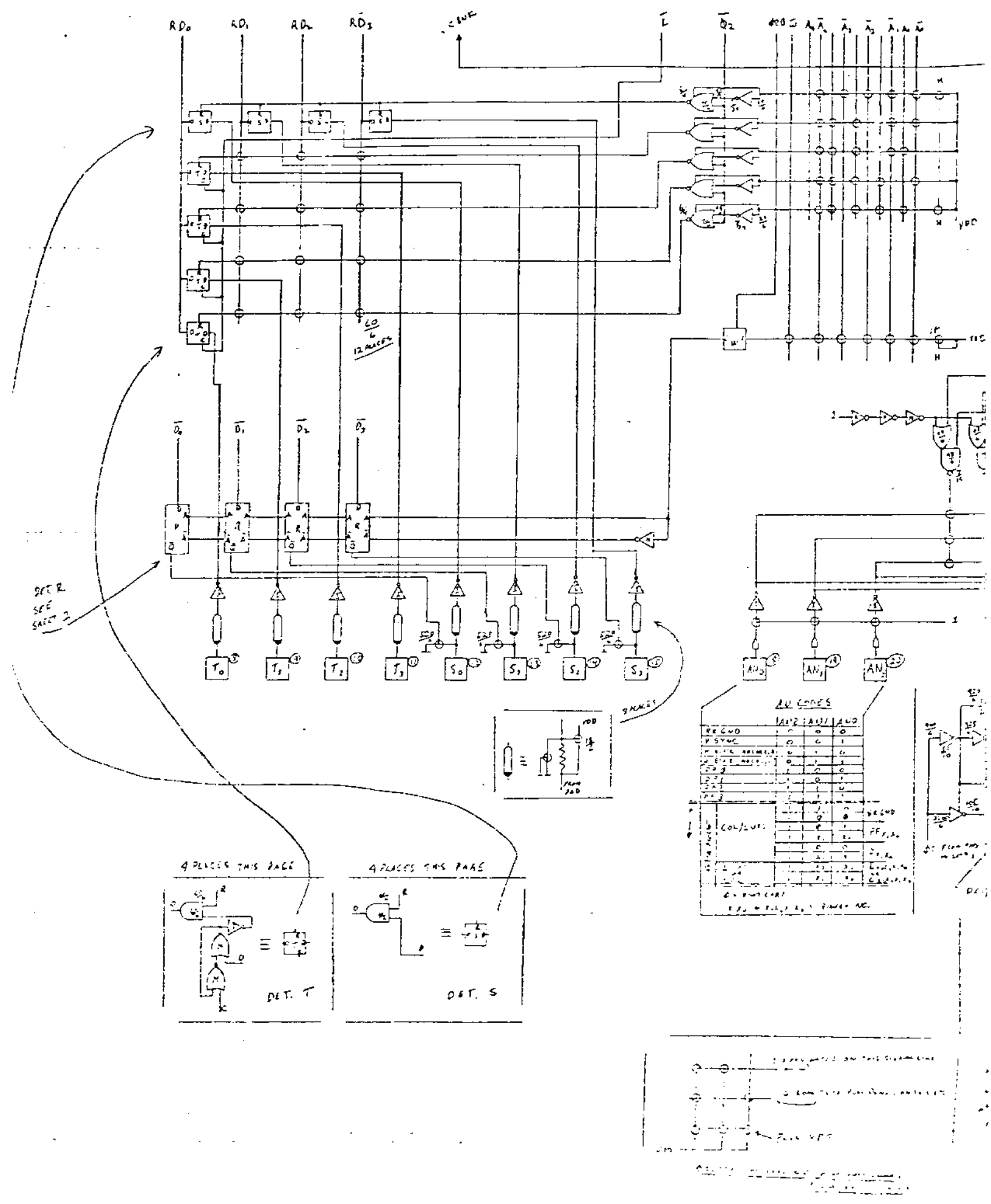
SHEET 32 OF 34

DRAWING NO C014805 | SHEETS 34 | REV A

4 | 3 | 2 | 1


RD0
RD1
RD2
RD3
SEE SHEET 2
4 PLACES THIS PAGE
4 PLACES THIS PAGE
DET. T
DET. S
AN CODES
12 PLACES
9 PLACES