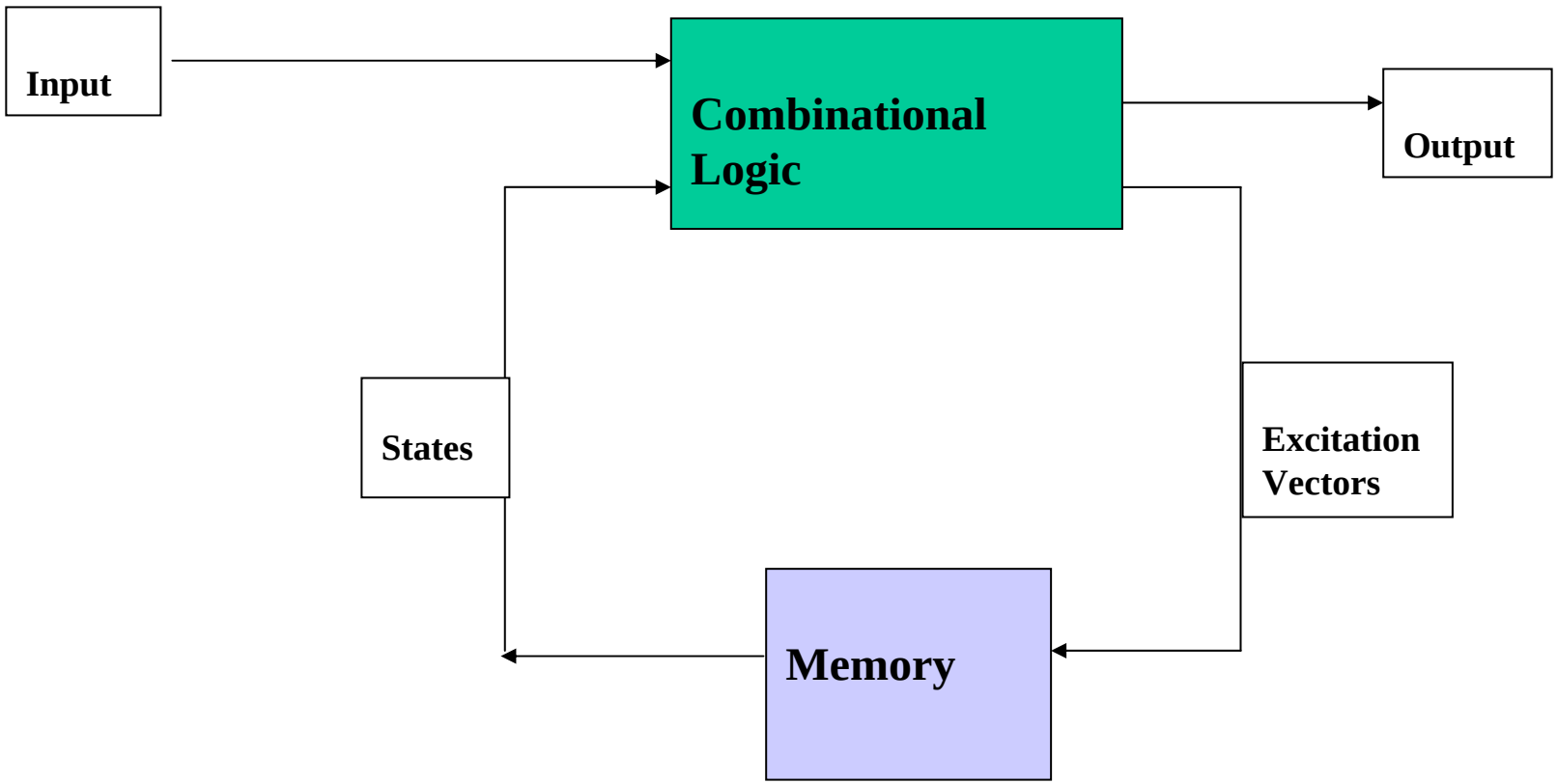
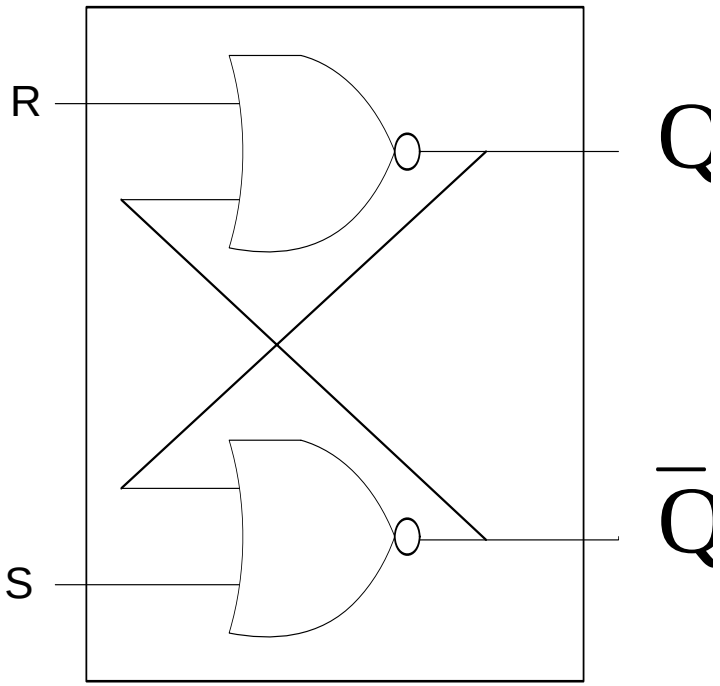

Input
Combinational Logic
Output
States
Excitation Vectors
Memory

RS Latch

$Q+ = S + R' Q$

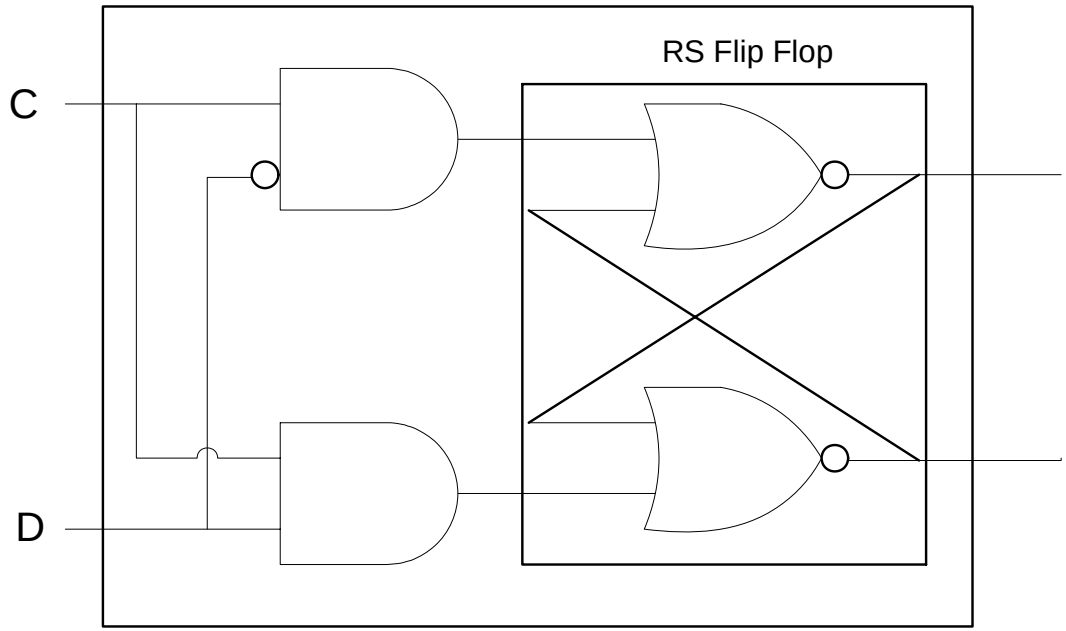


R	S	Q_{t+1}
0	0	$\bar{q}_t$
0	1	1
1	0	0
1	1	—

Two Problems:

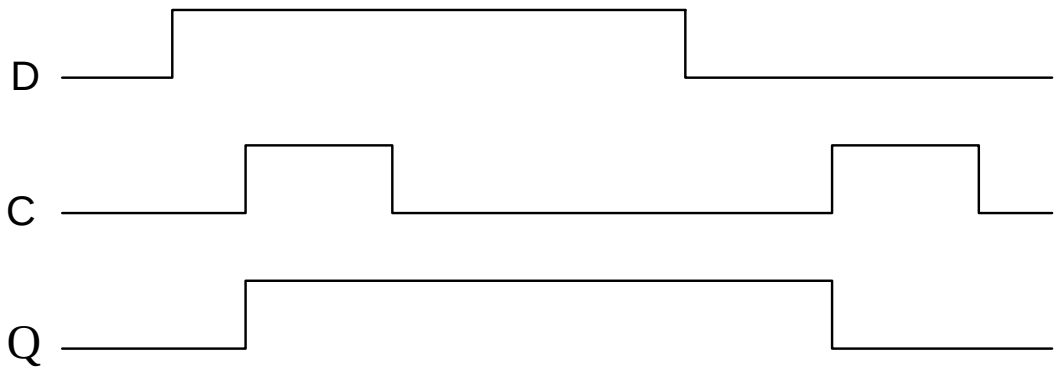
R=S= 1 Not allowed, Data is transparent

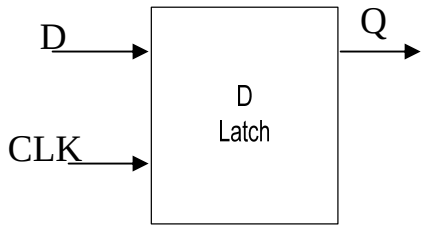
The D Latch



D	Q+
0	0
1	1

$Q^+ = D$



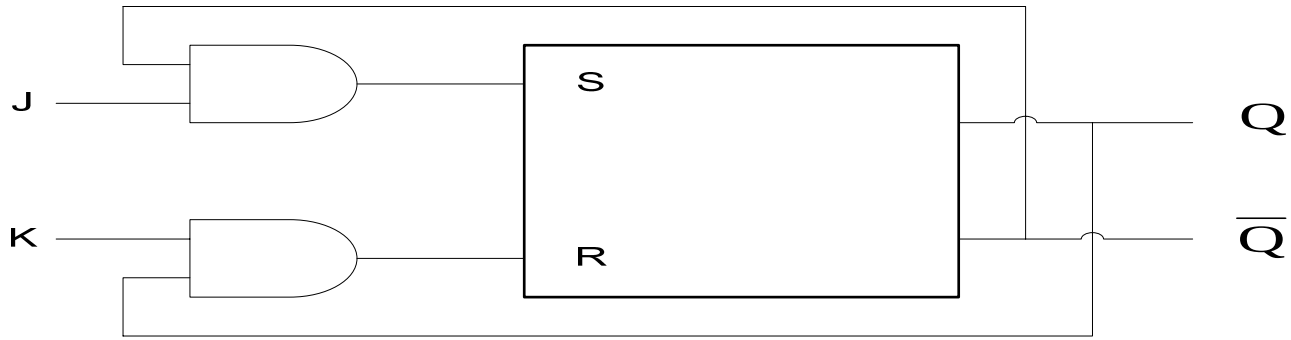


Problem: Level sensitive

JK Latch : Universal, Level sensitive,

Timing Constraints due to feed back.

JK Flip Flop:



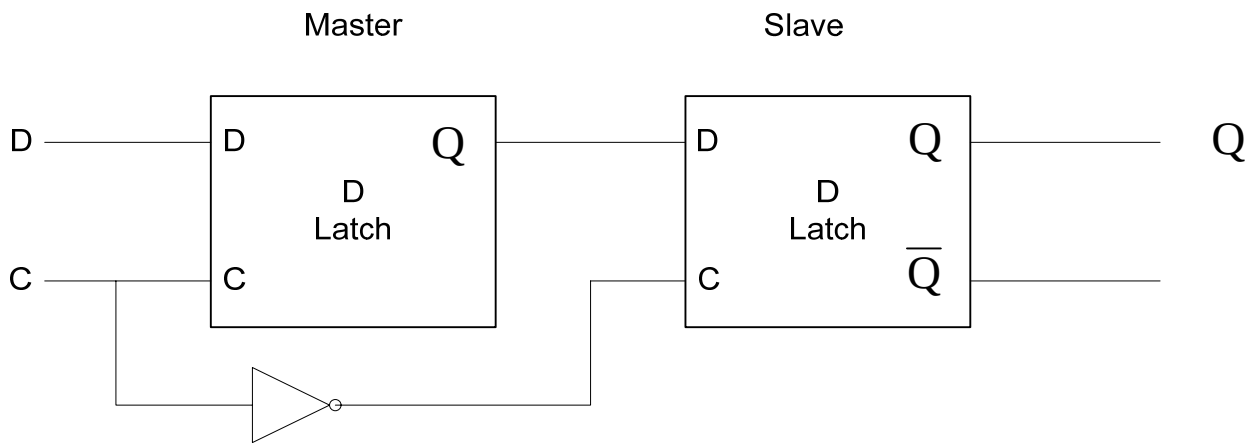
$$Q_{t+1} = J\overline{Q}_t + \overline{K}Q_t$$

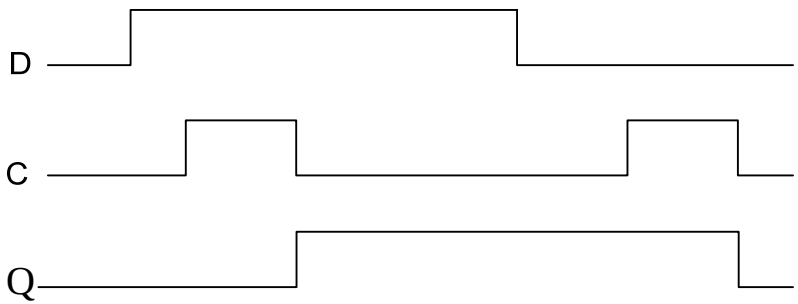
Master Slave Flip Flop

Edge sensitive,Set up and Hold time

Master and Slave Flip Flop :

A D Flip Flop with a falling-edge trigger.





Master Slave Flip Flop Edge sensitive,-Falling Edge

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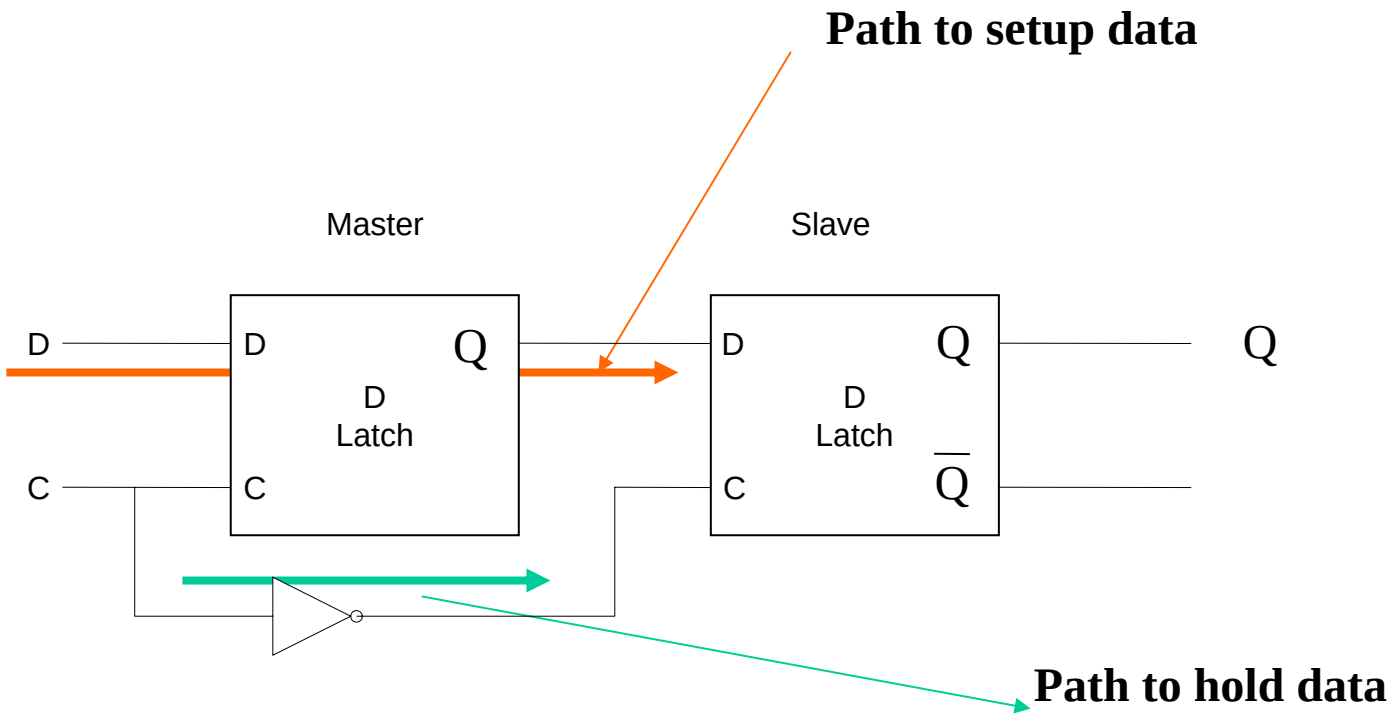
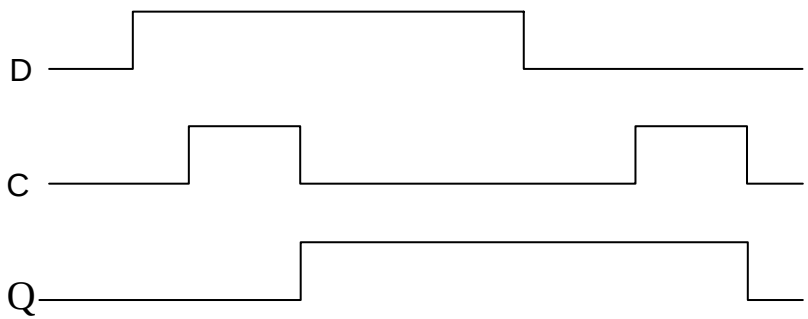
Set Up and Hold Time constraints





Edge triggered Flip Flop:

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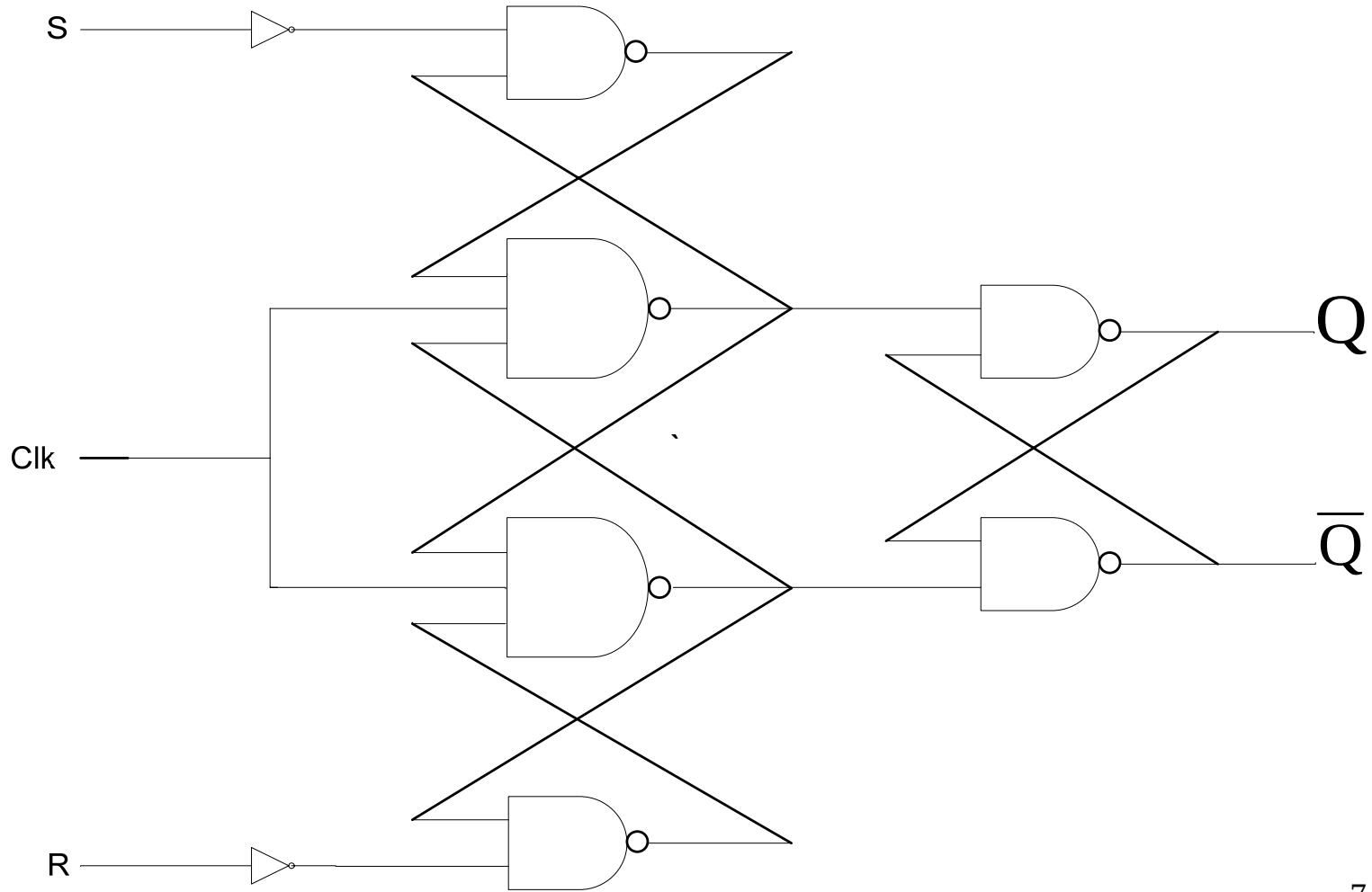
Set up and Hold time Constraints



Edge Triggered, D Flip Flop,

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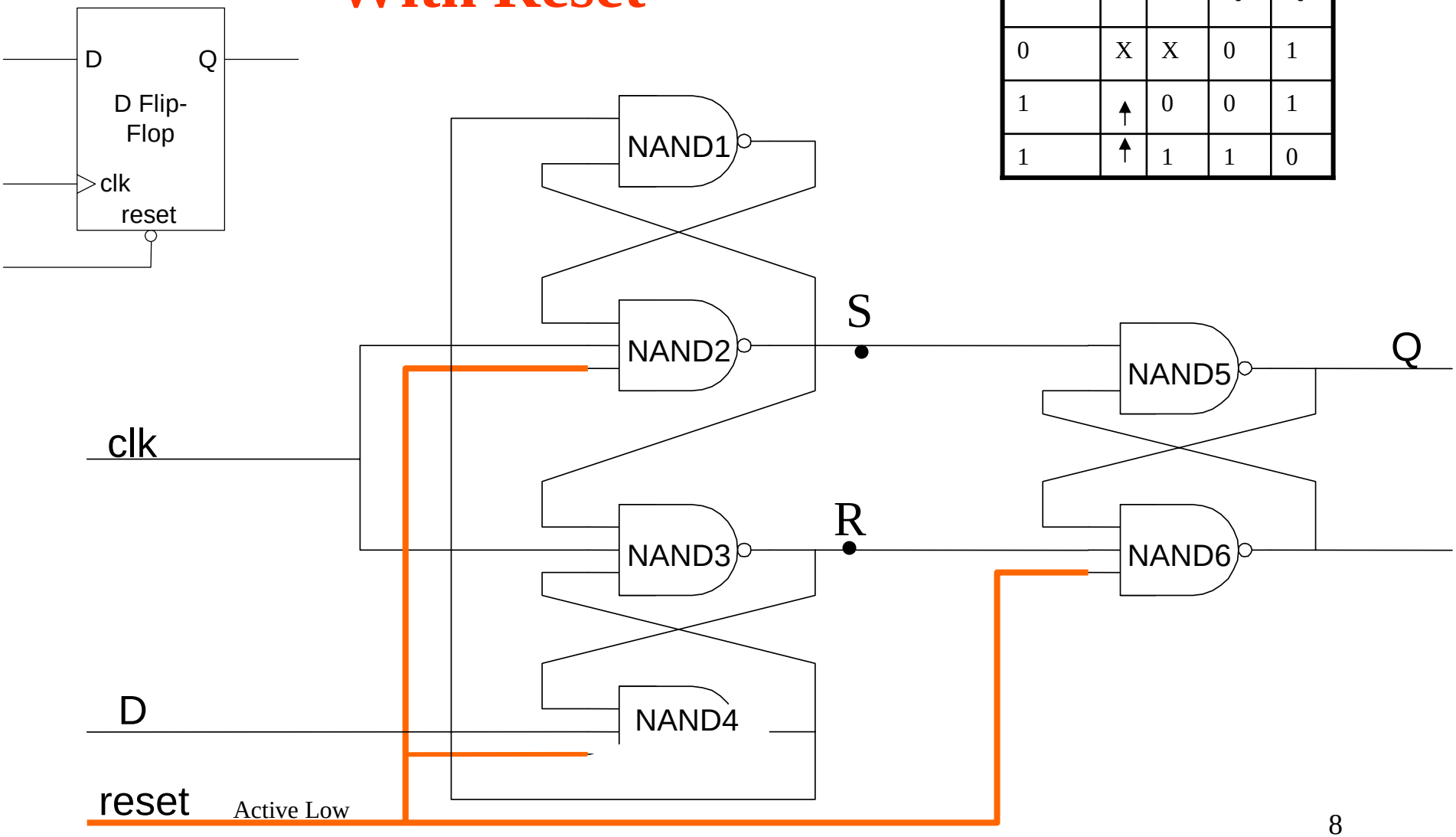
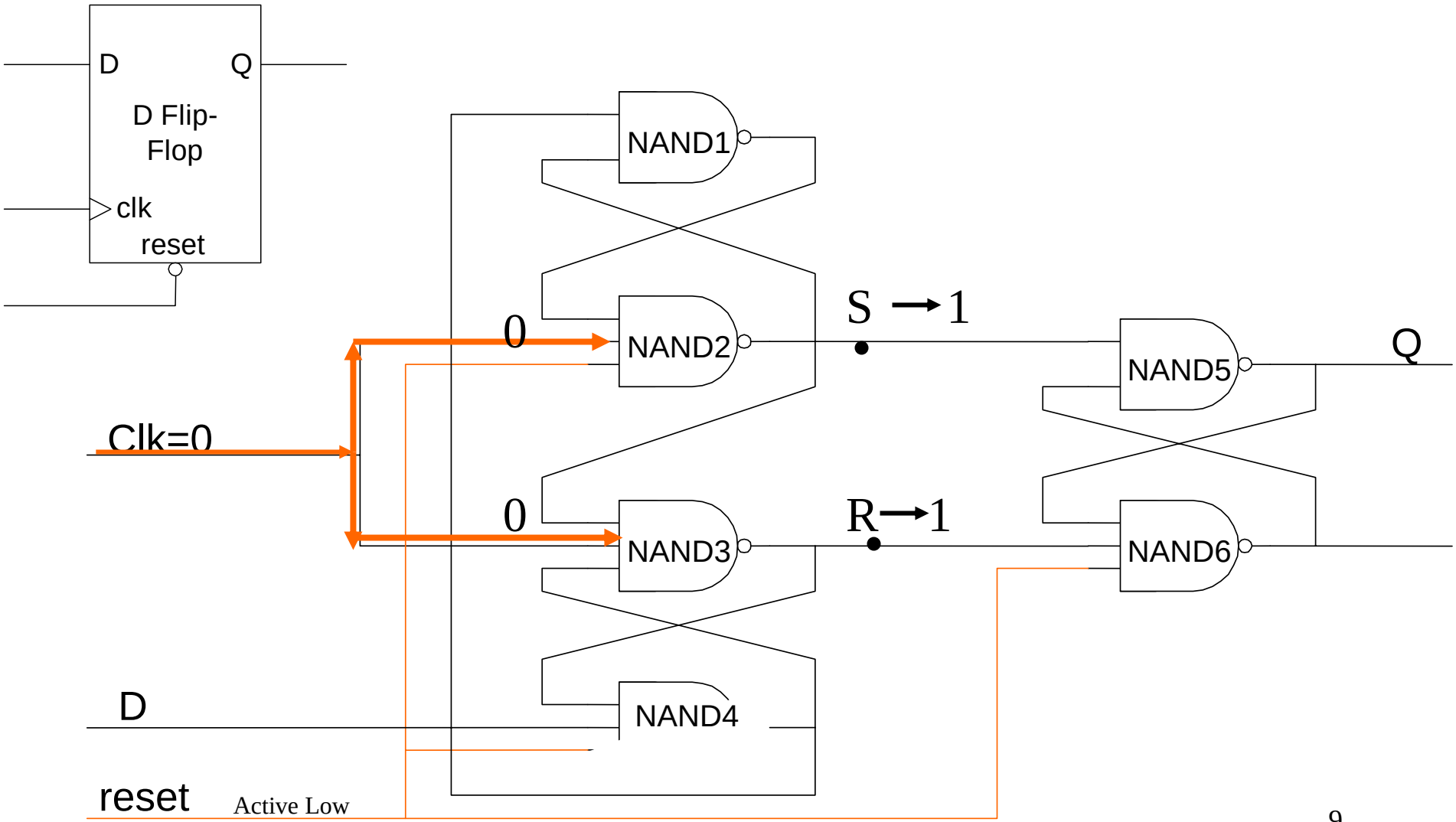
With Reset

Reset	C	D	Q	Q'
0	X	X	0	1
1	↑	0	0	1
1	↑	1	1	0



Edge Triggered, D Flip Flop

When CLK=0



When CLK changes from 0 to 1

Case1, D=0: t_{setup}= t4, t_{hold}=t3

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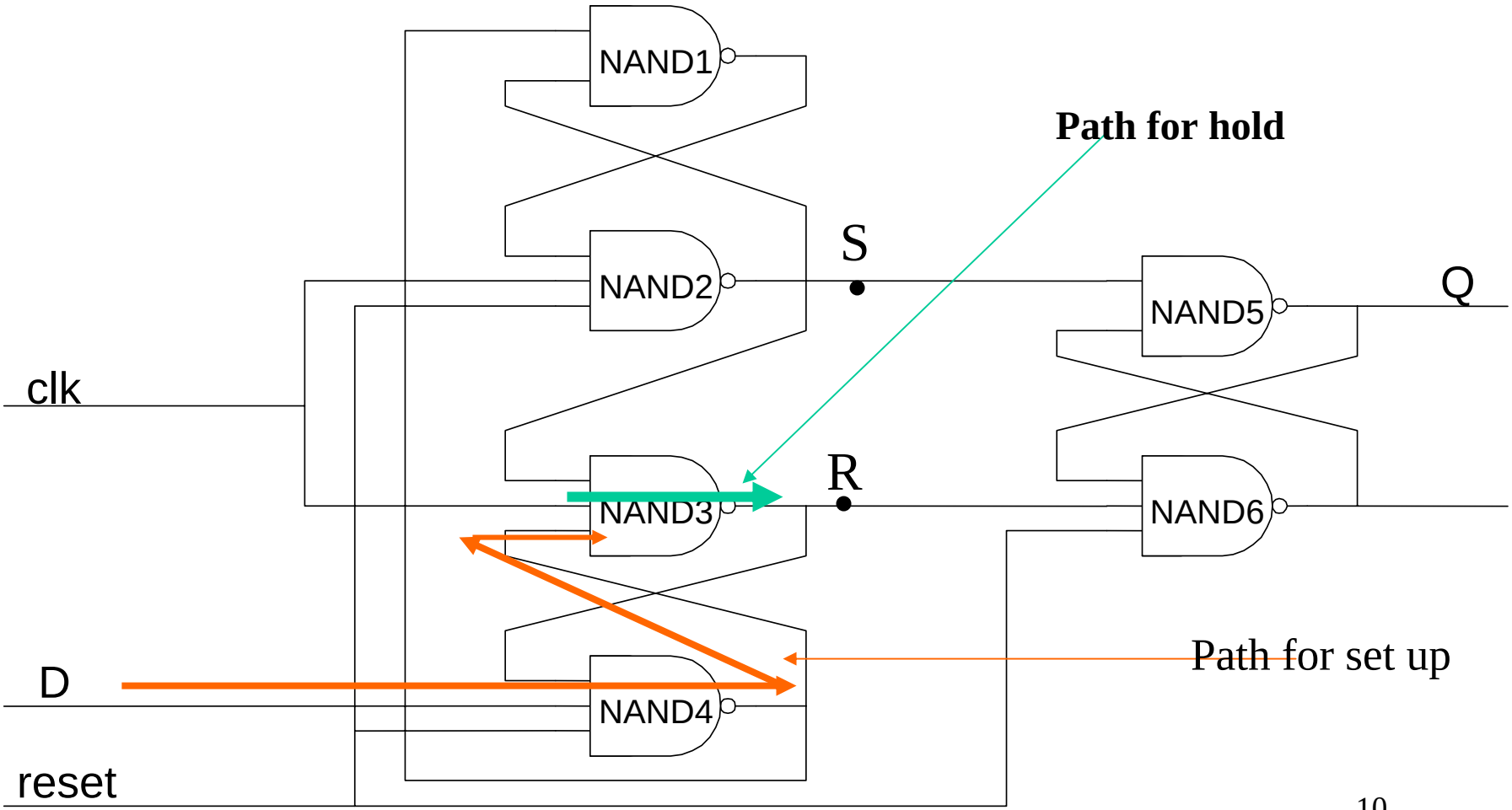

When CLK changes from 0 to 1

Case2, D=1 t_{setup}=t4 + t1 t_{hold}= t2

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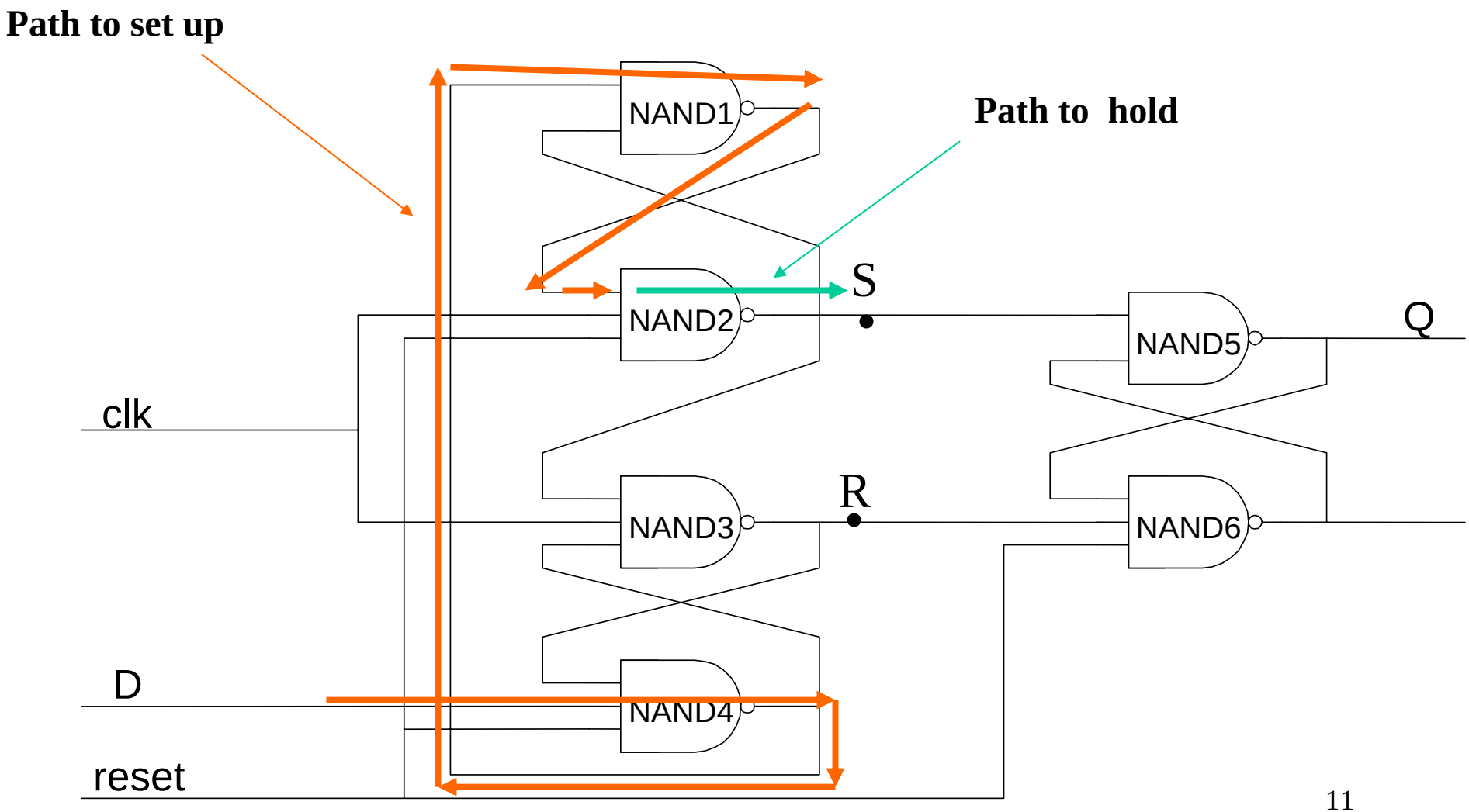
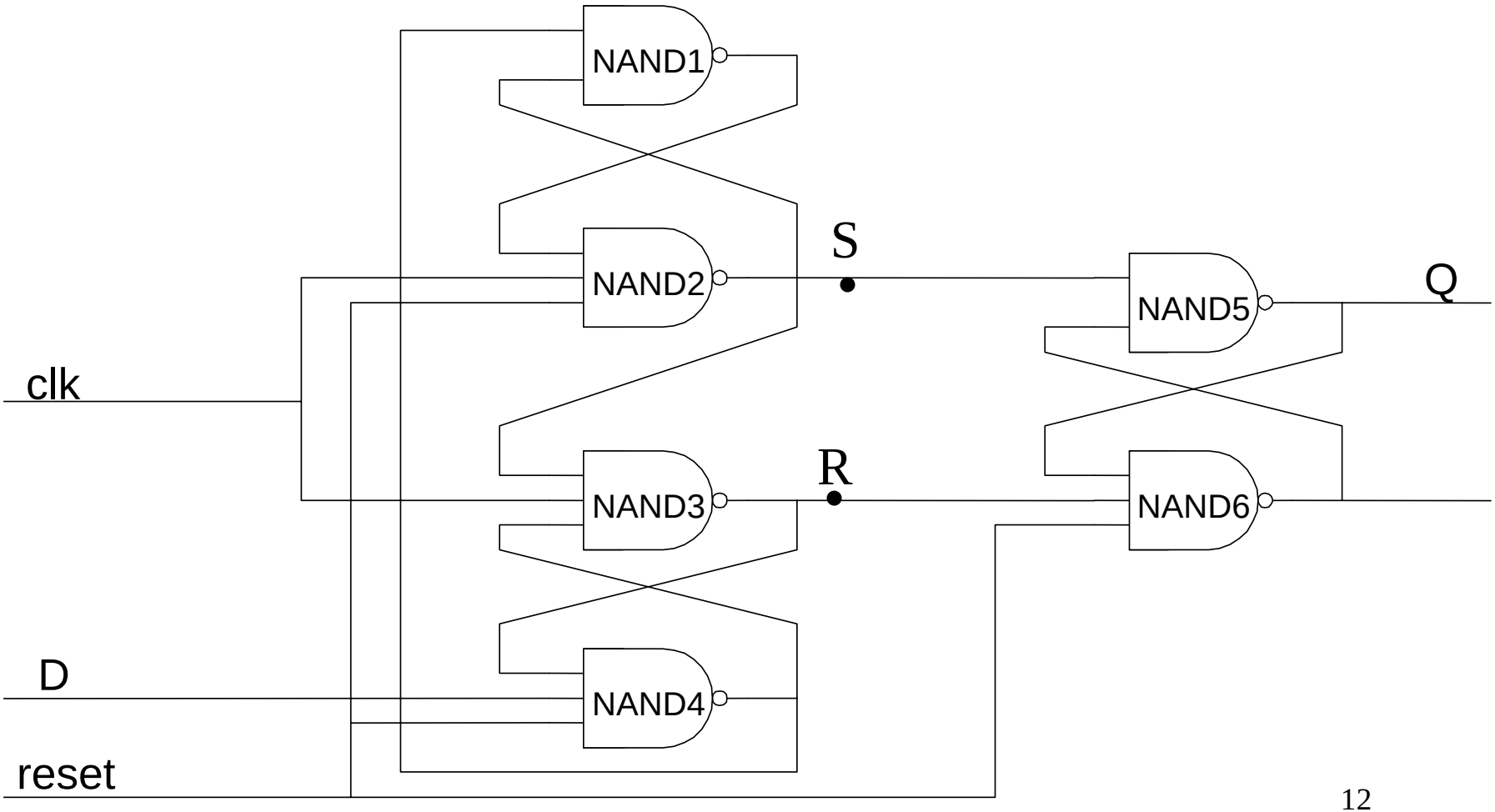


When CLK changes from 0 to 1

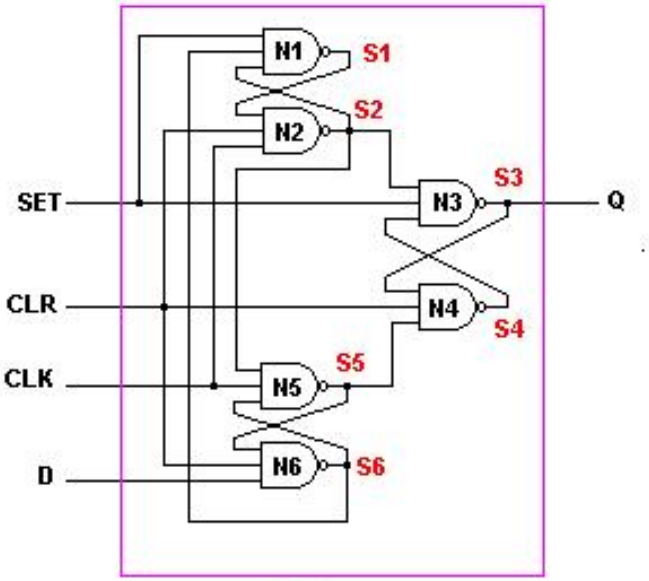
Case1, D=0: t_{setup}= t4, t_{hold}=t3

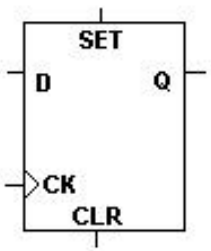
Case2, D=1 t_{setup}=t4 + t1 t_{hold}= t2

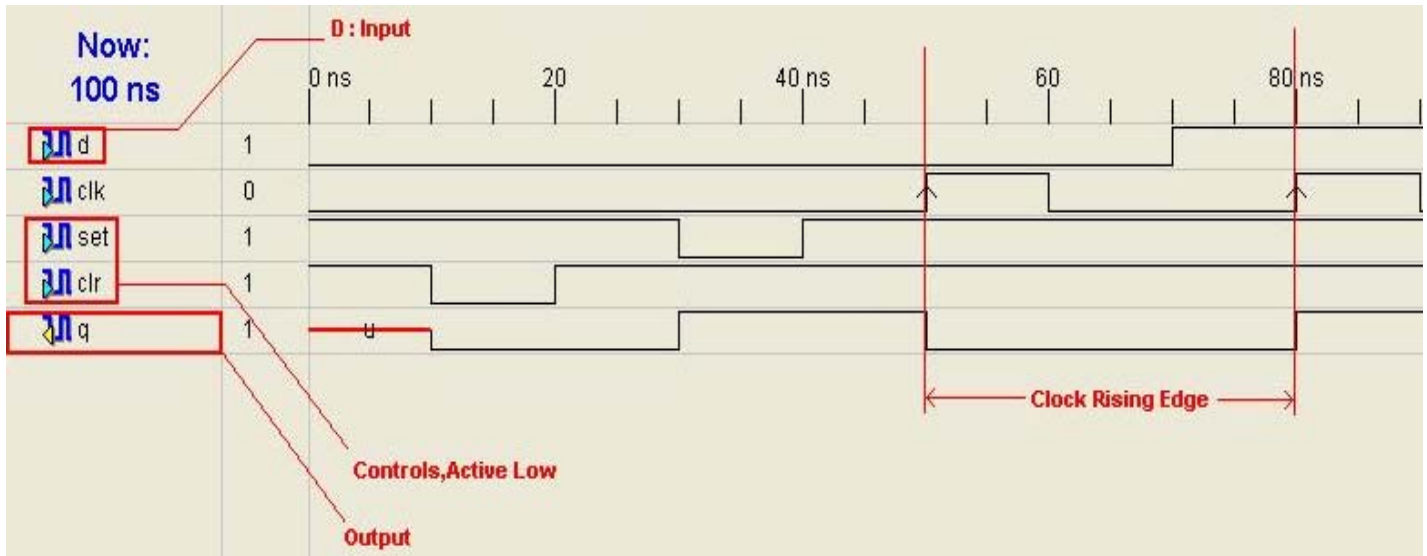


D Flip Flop

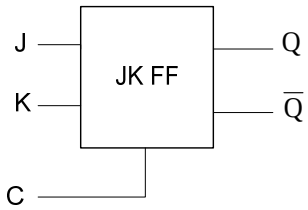
Concordia University

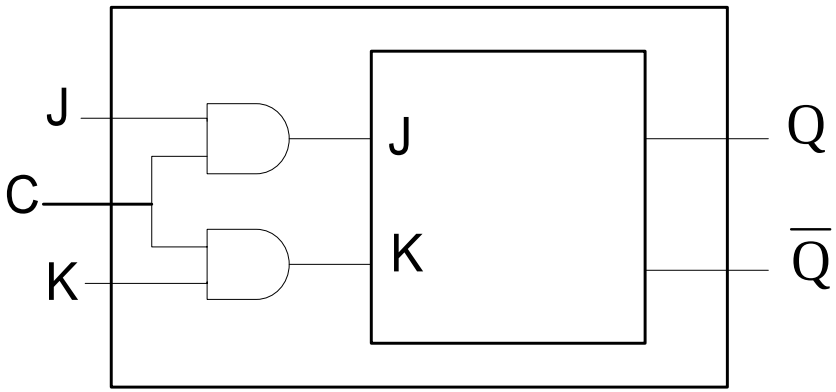






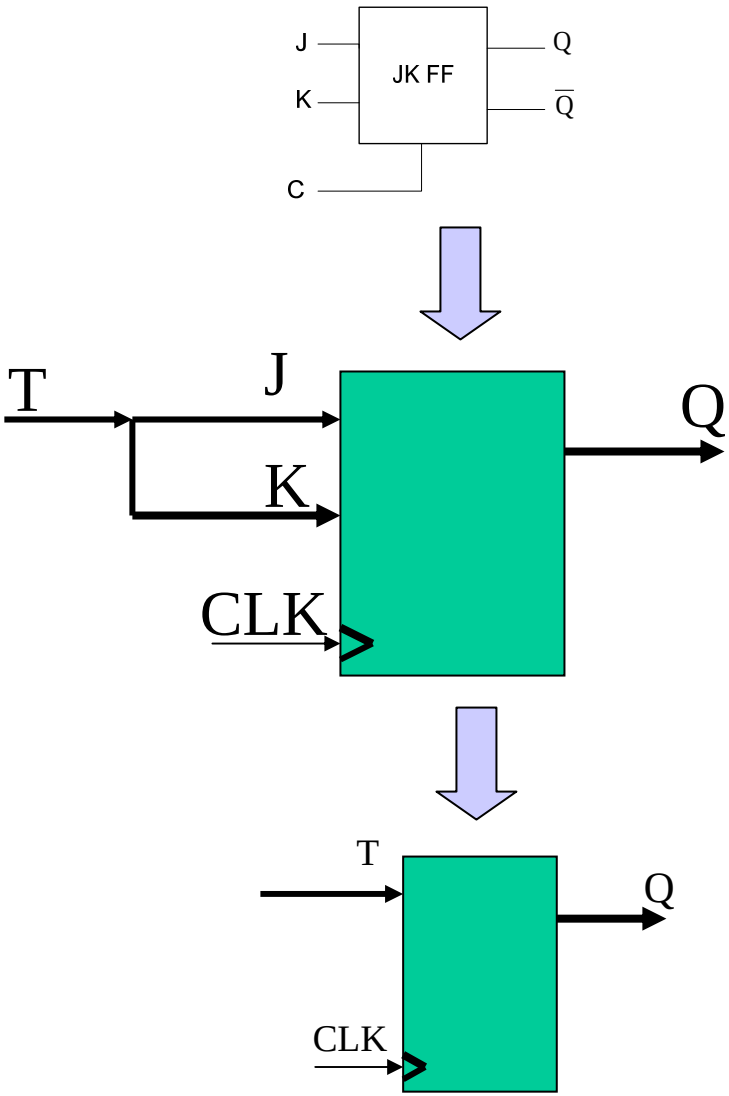
JK Flip Flop with a rising-edge :





$$Q^{+} = JQ' + K'Q$$

T-Flip Flop



$Q^+ = JQ' + K'Q$

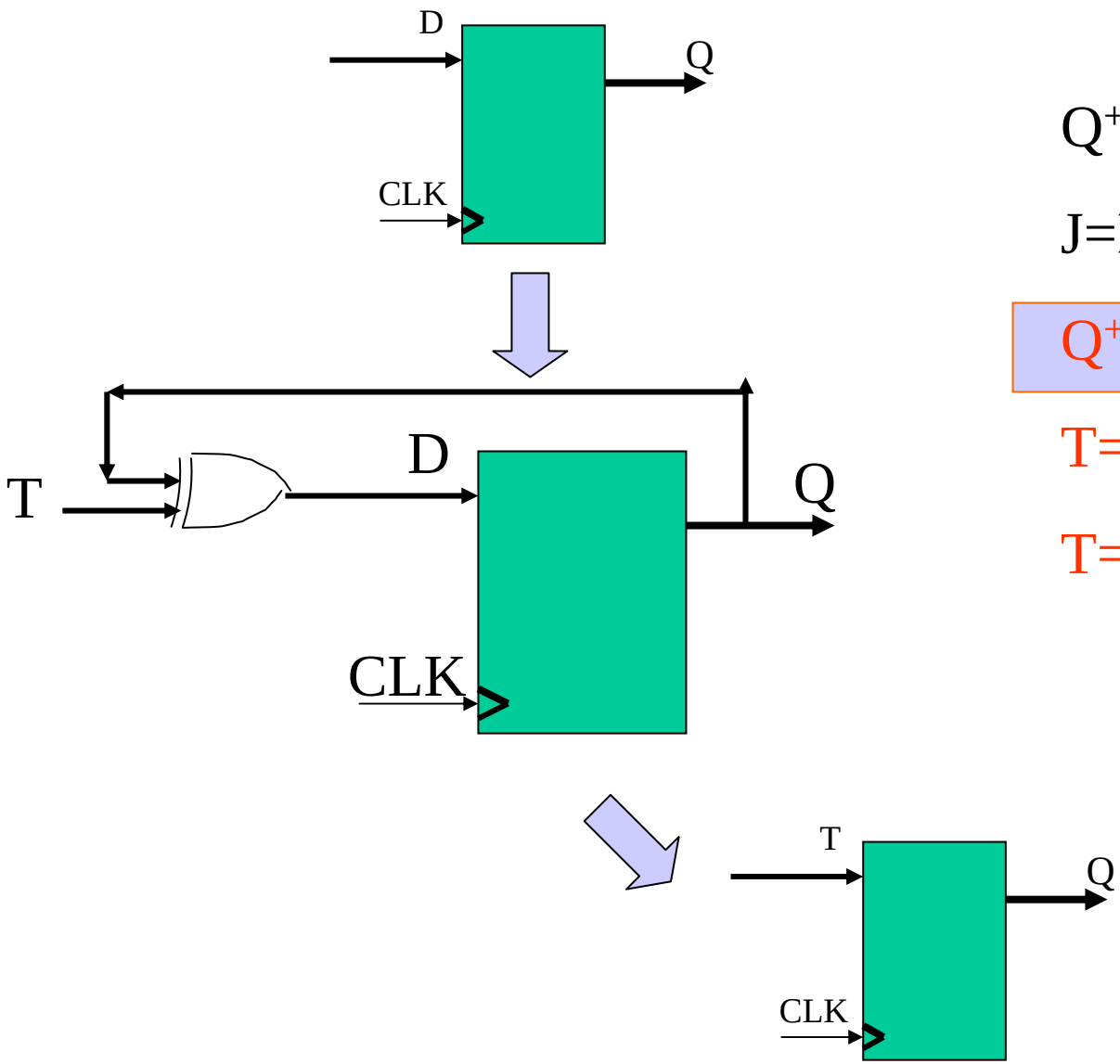
$J=K=T$

$Q^+ = TQ' + T'Q$

$T=1 \quad Q^+ = Q'$

$T=0 \quad Q^+ = Q$

T-Flip Flop



$Q^+ = JQ' + K'Q$

$J=K=T$

$Q^+ = TQ' + T'Q$

$T=1 \quad Q^+ = Q'$

$T=0 \quad Q^+ = Q$