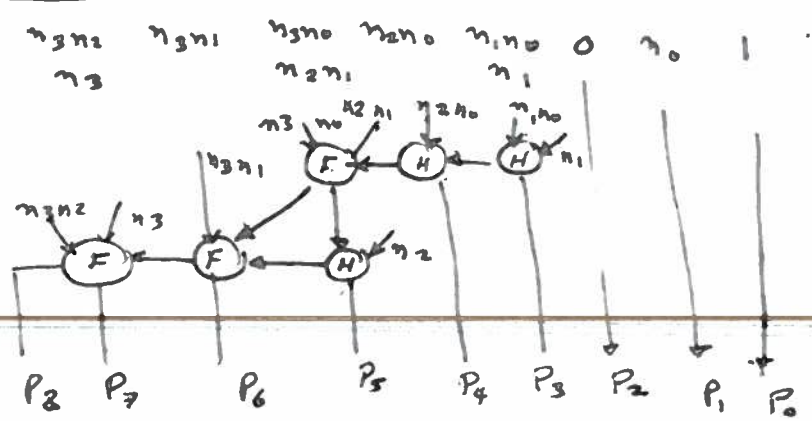


Q1

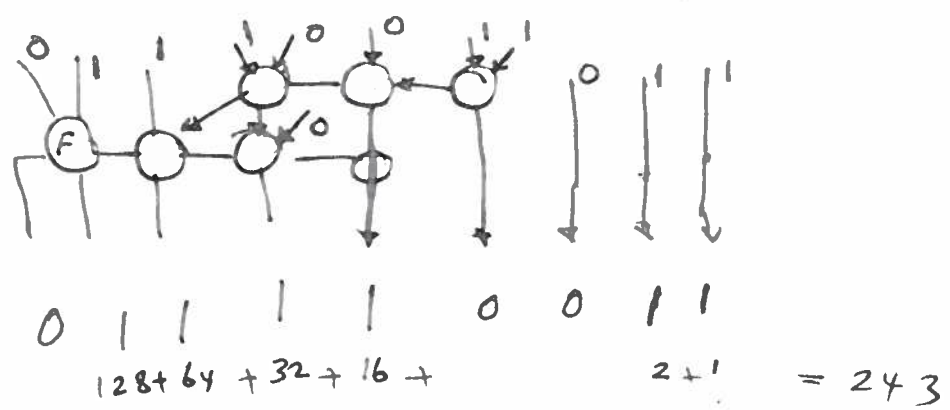
$$N = \begin{matrix} n_3 & n_2 & n_1 & n_0 \\ n_3 & n_2 & n_1 & n_0 \end{matrix}$$

$$\begin{matrix} n_3n_0 & n_2n_0 & n_1n_0 & n_0n_0 \\ n_3n_1 & n_2n_1 & n_1n_1 & n_0n_1 \\ n_3n_2 & n_2n_2 & n_1n_2 & n_0n_2 \\ n_3n_3 & n_2n_3 & n_1n_3 & n_0n_3 \end{matrix}$$

$$\begin{matrix} n_3n_2 & n_3n_1 & n_3n_0 & n_2n_0 & n_1n_0 & 0 & n_0 & 0 & \swarrow 2N^2 \\ n_3 & & n_2n_1 & & n_1 & & & & 1 & + & 1 \end{matrix}$$

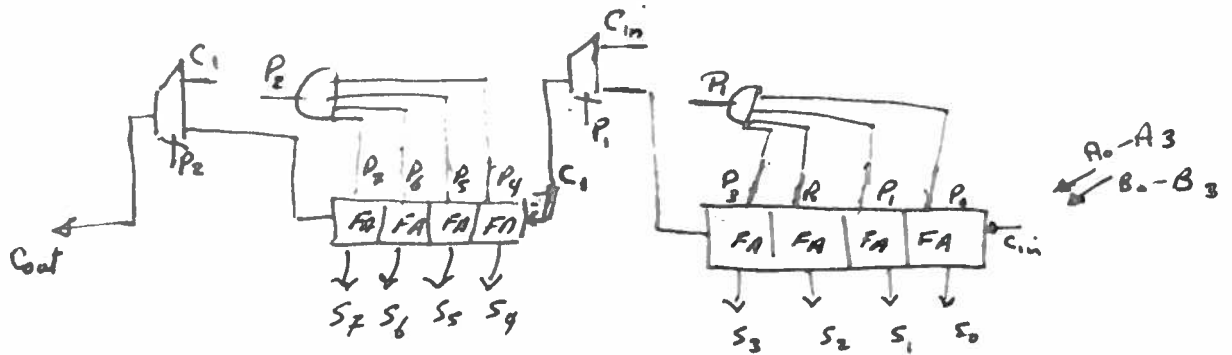


$$N = 1011 = 11 \quad 2N^2 + 1 = 243$$



Q 2

This implementation can be done in several ways, in terms of how to divide the 8-bit. Below we give implementation by using two 4-bit carry skip Adder

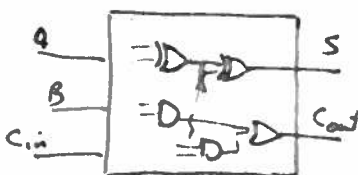


Critical Path  
Carry skip =  $8 * \tau_{FA} + 2 \tau_{AND} + 2 \tau_{MUX} = 8 * 3 + 2 \tau_{gate} + 3 * 2 \tau_{gate}$   
 $= 32 \tau_{gate}$

Critical Path  
Carry Ripple =  $8 * \tau_{FA} = 8 * 3 = 24 \tau_{gate}$

Area of Carry skip =  $8 * A_{FA} + 2 A_{AND} + 2 A_{MUX}$   
 $= 8 * 5 A_{gate} + 2 A_{gate} + 2 * 3 A_{gate}$   
 $= 48 A_{gate}$

Area of Carry Ripple =  $8 * A_{area FA}$   
 $= 8 * 5 A_{gate} = 40 A_{gate}$



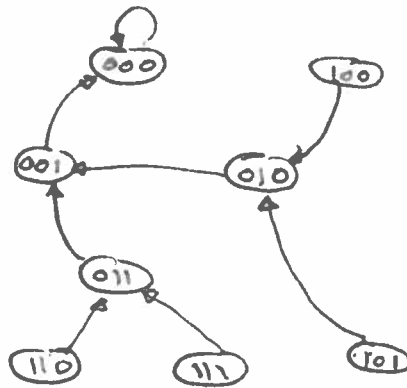
Full Adder  
 Delay =  $3 \tau_{gate}$   
 Area =  $5 A_{gate}$



Mux  
 Delay  $3 \tau_g$   
 Area =  $4 \tau_g$   
 neglect inverter

Q3

Oct 2012



Present state			Next state		
$y_3$	$y_2$	$y_1$	$y_3^+$	$y_2^+$	$y_1^+$
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	0	0	1
0	1	1	0	0	0
1	0	0	0	0	0
1	0	1	0	1	1
1	1	0	0	1	0
1	1	1	0	1	1

$y_3$	$y_2$	$y_1$	$y_3^+$	$y_2^+$	$y_1^+$
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	0	0	1
0	1	1	0	0	0
1	0	0	0	0	0
1	0	1	0	1	1
1	1	0	0	1	0
1	1	1	0	1	1

$y_1^+ = y_2 = D_1$

$y_3$	$y_2$	$y_1$	$y_3^+$	$y_2^+$	$y_1^+$
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	0	0	1
0	1	1	0	0	0
1	0	0	0	0	0
1	0	1	0	1	1
1	1	0	0	1	0
1	1	1	0	1	1

$y_2^+ = y_3 = D_2$

$y_3$	$y_2$	$y_1$	$y_3^+$	$y_2^+$	$y_1^+$
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	0	0	1
0	1	1	0	0	0
1	0	0	0	0	0
1	0	1	0	1	1
1	1	0	0	1	0
1	1	1	0	1	1

$y_3^+ = 0 = D_3$

Using D Flip Flop

$y_3^+ = 0 = D_3$   
 $y_2^+ = y_3 = D_2$   
 $y_1^+ = y_2 = D_1$

