

SSN: _____ (no names please)

Work all problems.

1. (8 pts) Plot the following function on a K-Map.

$$F(A,B,C,D) = AD + B\bar{C}$$

		AB			
		00	01	11	10
CD	00				
	01				
	11				
	10				

2. (8 pts) Plot the following function on a K-Map.

$$F(A,B,C,D) = \prod M(0,3,4,8,12,13,15)$$

		AB			
		00	01	11	10
CD	00				
	01				
	11				
	10				

3. (8 pts) Simplify the following K-map to get a **minimal SOP** form.

		AB			
		00	01	11	10
CD	00				
	01				
	11				
	10				

4. (8 pts) Simplify the following K-Map to get a **minimal POS** form.

		AB			
		00	01	11	10
CD	00				
	01				
	11				
	10				

5. (8 pts) On the diagram below, I want Y to be asserted (LOW TRUE) when both switches are depressed. Draw the Gate(s) that I need. Be sure to list the GATE NUMBERS (i.e. 7400, 7402, etc).

6. (8 pts) On the following map, identify a PRIME IMPLICANT, an ESSENTIAL PRIME IMPLICANT, and a NON-ESSENTIAL Prime Implicant.

		AB			
		00	01	11	10
CD	00				
	01				
	11				
	10				

7. (10 pts) a. I would like to implement one function $F(A,B,C)$ and one function $G(W,X,Y,Z)$ in the same memory device. Note that the two functions do not share any common variables. What size memory device do I need? (specified as $K \times M$, where K is the number of locations, M is the number of bits per location).

b. I would like to implement the function $F(A,B,C)$, $G(B, C, D)$, and $H(C, D,E)$ in the same memory device. Note that the three functions share some common variables. What size memory device do I need? (specified as $K \times M$, where K is the number of locations, M is the number of bits per location)

8. (5 pts) On the attached PLD diagram (Figure 1), explain what function is implemented according to the fuse marking.

$$Y' = \text{?????}$$

9. (5 pts) Write the following function in SOP form using the minterms indicated. Do NOT minimize.

$$F(A,B,C,D) = \sum m(3,5,15)$$

10. (5 pts) Write the following function in POS form using the maxterms indicated. Do NOT minimize.

$$F(A,B,C,D) = \prod M(3,5,15)$$

11. (15 pts) For the PLD diagram labeled as "Figure 2", answer the following questions:

- a. What is the maximum number of logic equations I could implement in this PLD at the same time?
- b. What is maximum number of input variables that equation could have?
- c. What is the maximum number of product terms each equation could have? (assuming that an output is NOT fed back around to an input).
- d. Show how to implement the equation (do NOT attempt to minimize this equation, implement as shown):

$$Y(A,B,C,D,E,F,G,H) = A'B + ACE' + FG' + D'G'H'$$

12. Fill in the blanks using terms from the following list:

INEFFICIENT, Volatile, 1, JEDEC, Non-Volatile, 0, VHDL, EFFICIENT, PLD, PRODUCT TERM, Memory, LookUp Table, Intact, Fuse, POS, SOP, Non-Intact

- a. When all fuses are intact, the value of a product term in a PAL is _____ .
- b. A memory is _____ at implementing wide Boolean functions and multiple functions of independent variables.
- c. A _____ File specifies which fuses should be blown or left intact within a PLD.
- d. A PLD which must be reconfigured (reprogrammed) on every power up has _____ programming.
- e. Another name for a memory is _____ when it is used to implement a combinational function.
- f. _____ is a language used for specifying boolean equations which can be mapped to programmable logic.