4 Logic Gates

This experiment will introduce **AND**, **OR**, **NAND**, **NOR** and **Exclusive OR** logic gates. You will learn about:

- Electrical characteristics of logic circuits.
- Operation of basic gates.
- The concept of a **universal gate**.
- The power of **two-level logic**.
- The use of multiple levels to expand gate inputs.

I. Prelab

You must have this information when you ENTER THE LAB.

A. Use the TTL Logic Data Book to locate the following information.

1. Define t_{PHL} and t_{PLH}.
2. Locate the datasheets for the following parts: 74LS08, 74LS00, 74LS32, 74LS02, 74LS86.
   a. Create a table that shows the TYPICAL delay values for t_{PHL} and t_{PLH} for each gate.
   b. There are more delay values for the 74LS86 than there are for the other gate types. Why is this? EXPLAIN!
3. From the datasheet of the 74LS00:
   a. What is the minimum input voltage for a logic ‘1’?
   b. What is the minimum input voltage for a logic ‘0’?
   c. What is the minimum output voltage for a logic ‘1’?
   d. What is the minimum output voltage for a logic ‘0’?.
   e. Compute the difference (C – A), (D-B). Why must this be a positive number? Explain what a “noise margin” is and why it is important.

B. Prepare truth tables for each of this experiment's logic diagrams.

C. Label each of the logic diagrams with pin assignments using the TTL Data Book.

In future experiments you will be required to perform prelab assignments similar to those just listed. However, the procedures will not be given explicitly in your lab manual.

II. Procedure

……

A. Assemble the circuits in Figure 1 through Figure 5. Verify that each circuit operates as expected. Compare your results with those in your truth

tables.

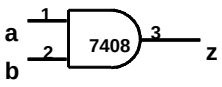

Figure 1 AND

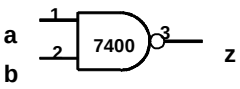

Figure 2 NAND

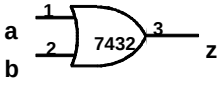

Figure 3 OR

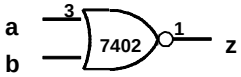

Figure 4 NOR

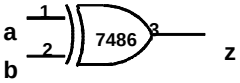

Figure 5 XOR

B. A universal gate is a logic gate that can be used to create all the basic logical functions. These two gates are the NAND and the NOR.

1. Connect the circuit in Figure 6 and verify that it operates as an inverter.
2. Connect the circuit in Figure 7 and verify that it operates as an inverter.
3. Connect the circuit in Figure 8 and verify that it operates as an OR gate.

Figure 6

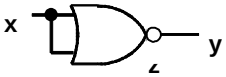

Figure 7

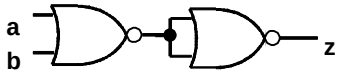

Figure 8

4. Assemble each of the circuits in Figure 9 through Figure 11 and determine the equivalent gate represented by each circuit.

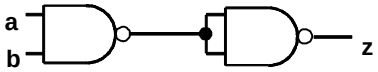

Figure 9

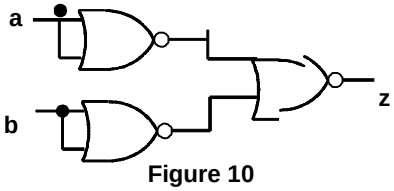

Figure 10

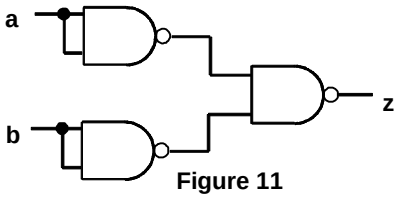

Figure 11

C. All combinational logic functions can be represented in sum-of-products (AND/OR) form and product-of-sums (OR/AND) form. This implies that all functions can be implemented in two levels of logic provided that at each level gates have enough inputs. In practice, this may not be realizable due to limitations on fan-in (maximum number of inputs a gate may have). It should also be noted that AND/OR and OR/AND forms can be converted to forms that use only the universal gates.

1. Assemble the circuits in Figure 12 and Figure 13 and show that the (AND/OR) form is equivalent to the (NAND/NAND) form.

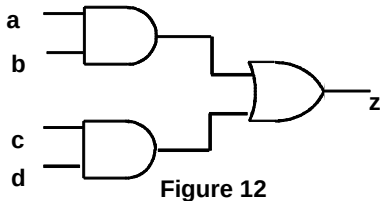

Figure 12

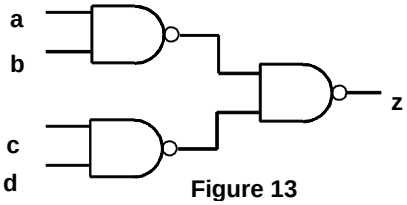

Figure 13

2. Assemble the circuits in Figure 14 and Figure 15 and show that the (OR/AND) form is equivalent to the (NOR/NOR) form.

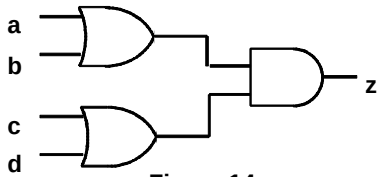

Figure 14

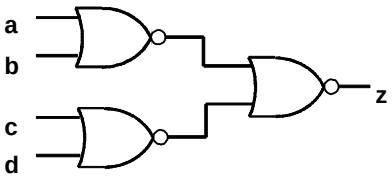

Figure 15

D. Fan-in can be increased using multiple levels of two-input gates

1. Connect the circuit in Figure 16 and show that it operates as a three-input AND gate.

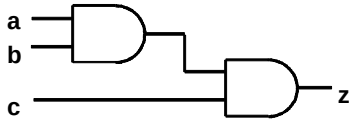

Figure 16

2. Assemble the circuits in Figure 17 and Figure 18 and determine which circuit operates as a three-input NAND gate.

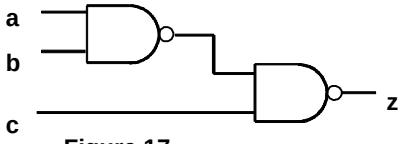

Figure 17

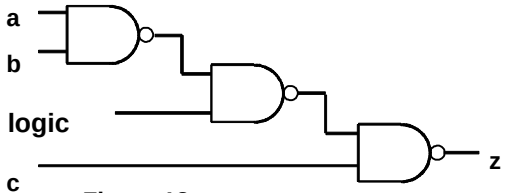

Figure 18

E. In logic circuits it is not always obvious that there is a time delay between the time an input changes and the time the output changes. This delay is known as propagation delay and it must be taken into account in many circuit designs.

1. Connect the circuit in Figure 19. Notice that the output appears to always be a logic `1' regardless of the input setting.

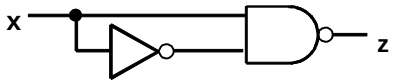

Figure 19

2. Connect the 1 Mhz digital clock output on the test box to the input of the circuit. Monitor the input to the circuit on CH1 of the scope and monitor the output of the circuit on CH2. Adjust the CH2 vertical scale in order to clearly see the `glitch' caused by propagation delay. Record all waveforms.

III. Report

……

A. Include Section II.B. Explain why a logic `1' can be used as one input to a NAND gate in order to use the gate as an inverter.

B. Include Section II.C.

C. Include Section II.E. Include accurate drawings of the waveforms. Explain these results.

PRE LAB DATA SHEET (THIS MUST BE FILLED OUT PRIOR TO LAB!!!)

TA CHECK OFF SIGNATURE:_____

A.1 Explain the concept of Tplh, Tphl. Draw a diagram to illustrate your point:

A.2 Gate Delay values:

Gate	Tplh	Tphl
74ls00		
74ls02		
74ls08		
74ls32		
74ls86 (case 1)		
74ls86 (case 2)		

Explanation of 74ls86 delay values (Draw diagrams to illustrate your point).

A.3

Gate	Voltage Values			
	VOH	VOL	VIH	VIL
7400				

VOH – VIH = _____

VOL – VIL = _____

Explanation of NOISE MARGIN:

Truth Tables:

Input		Output of Figure								
A	b	3.1	3.2	3.3	3.4	3.5	3.8	3.9	3.10	3.11
0	0									
0	1									
1	0									
1	1									

Input	Output of Figure		
X	3.6	3.7	3.19
0			
1			

Input				Output of Figure			
a	**b**	**c**	**d**	**3.12**	**3.13**	**3.14**	**3.15**
0	0	0	0				
0	0	0	1				
0	0	1	0				
0	0	1	1				
0	1	0	0				
0	1	0	1				
0	1	1	0				
0	1	1	1				
1	0	0	0				
1	0	0	1				
1	0	1	0				
1	0	1	1				
1	1	0	0				
1	1	0	1				
1	1	1	0				
1	1	1	1				

Input			Output of Figure		
a	**b**	**c**	**3.16**	**3.17**	**3.18**
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

LAB DATA SHEET (Record these values during lab!!!)

Truth Tables: TA CHECKOFF SIGNATURE: _____

Input		Output of Figure								
A	**b**	**3.1**	**3.2**	**3.3**	**3.4**	**3.5**	**3.8**	**3.9**	**3.10**	**3.11**
0	0									
0	1									
1	0									
1	1									

Input	Output of Figure	
X	**3.6**	**3.7**
0		
1		

Equivalent Gates: 3.9 = _____, 3.10 = _____, 3.11 = _____

Does figures (12,13) & (14,15) have the same results? _____

Input			Output of Figure		
a	**b**	**c**	**3.16**	**3.17**	**3.18**
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

Input x	Figure 3.19
0	
1	

(E) 1. Complete the circuit and obtain the logic result.
2. Use the 1 Mhz Clock as input to circuit figure 3.19
3. Connect CH1 to the input and CH2 to the output. Sketch both the input and output waveforms showing the propagation delay, period, pulse-width and voltage levels.