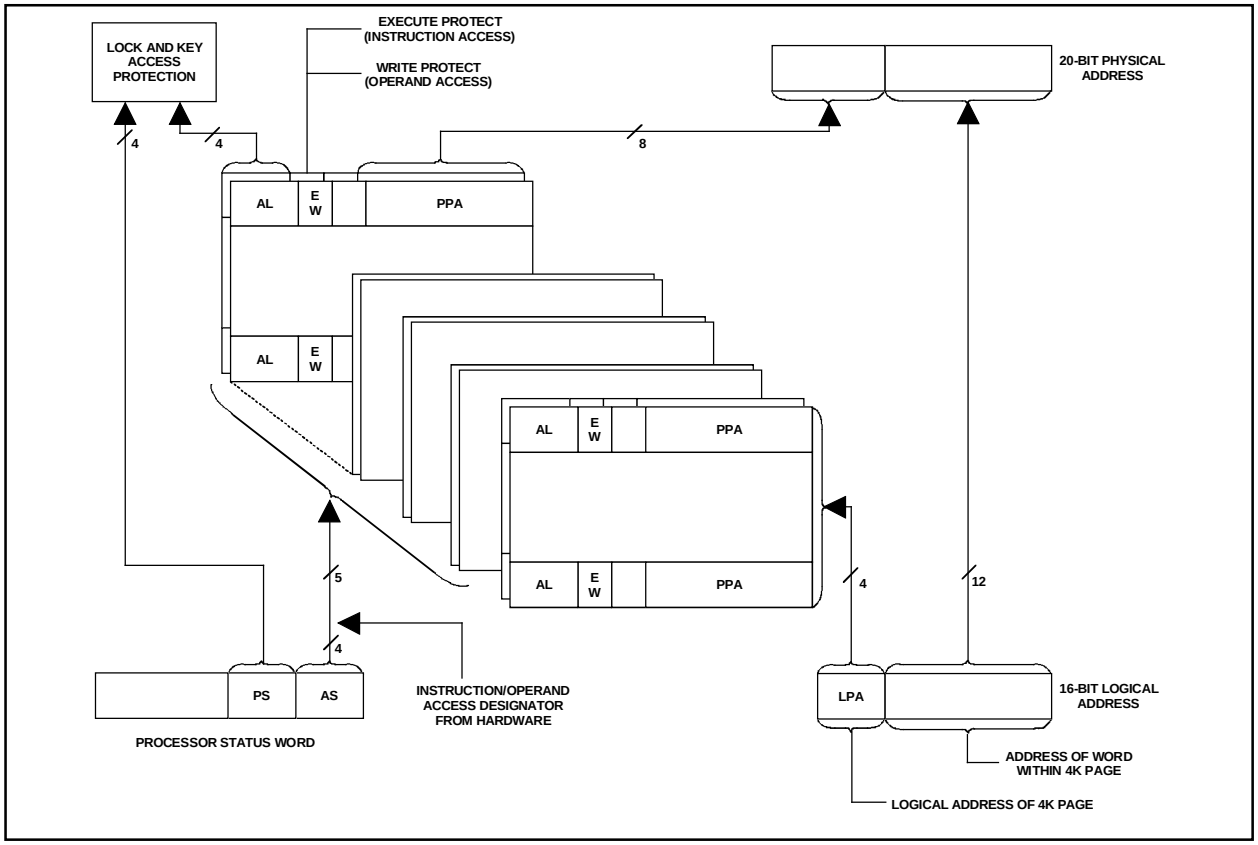
Memory Management Comparison 1750 versus ERC32

GMVSA 4003/98

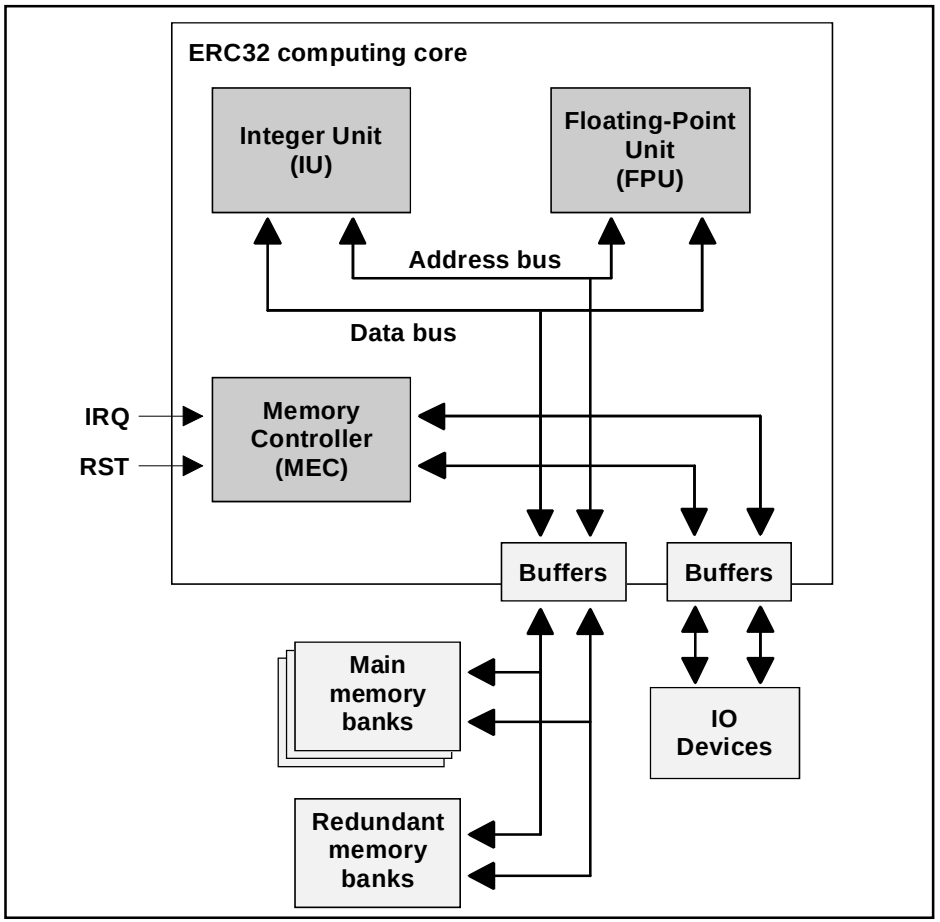
INTRODUCTION

- Objectives of the Study:
  - Comparison of the management of memory in computer systems based on 1750 with MMU versus ERC32 with MEC.
  - Memory Management problems can influence the software architecture: not generally foreseen.
  - Highlight the cost incurred in resolving problems rooted in the use of the 1750 MMU.

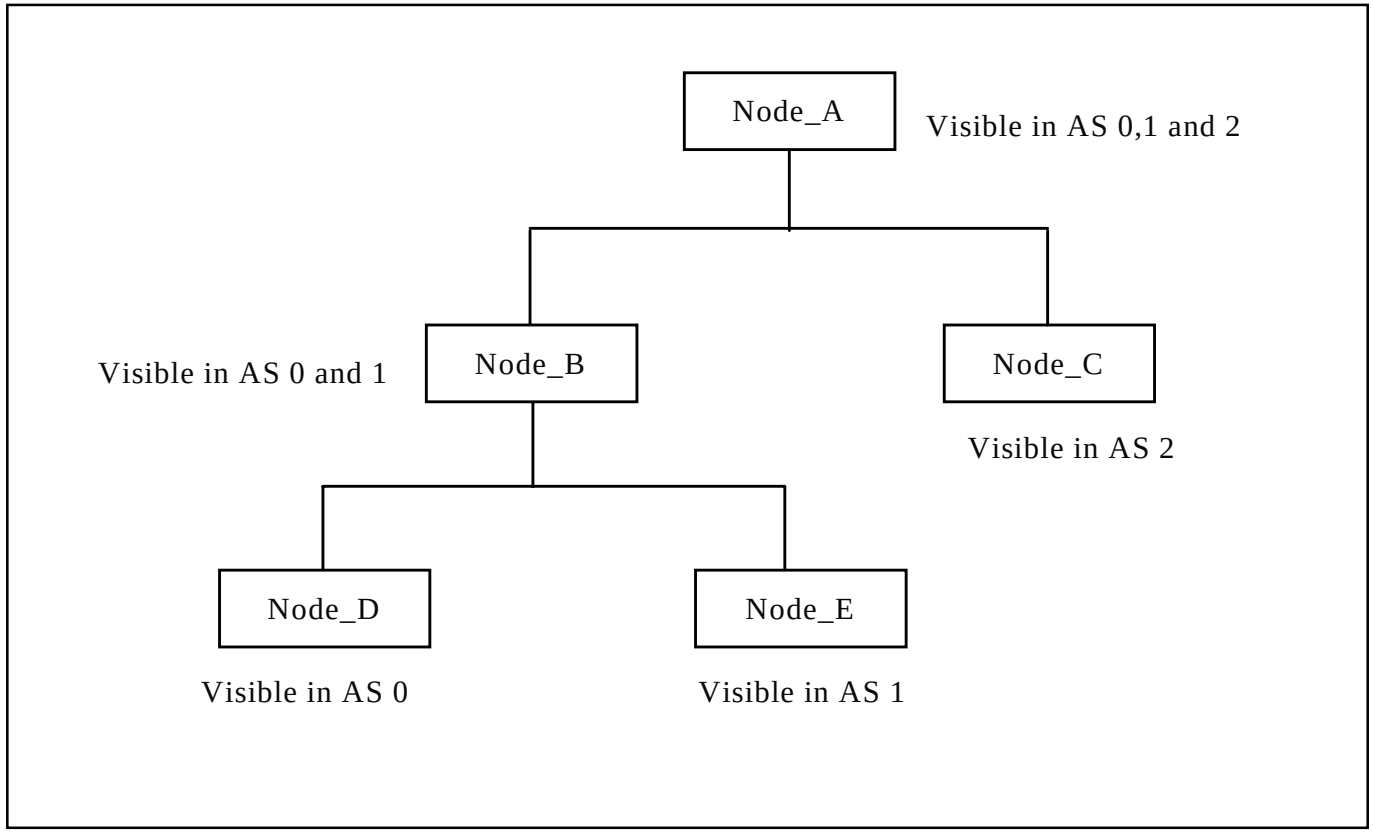
1750 Memory Management



ERC32 Memory Management



TLD's concept of "Nodes"



Typical 1750 Page Mapping

Address State 0

	Operand Pages	Instruction Pages
0	0	0
1	801	F
2	2	10
3	3	11
4	4	4
5	5	12
6	6	13
7	7	FFF
8	8	FFF
9	9	FFF
A	A	FFF
B	B	FFF
C	C	FFF
D	D	FFF
E	E	FFF
F	FFF	FFF

Address State 1

	Operand Pages	Instruction Pages
0	0	0
1	1	14
2	2	FFF
3	815	FFF
4	16	FFF
5	FFF	FFF
6	FFF	FFF
7	FFF	FFF
8	FFF	FFF
9	FFF	FFF
A	FFF	FFF
B	FFF	FFF
C	FFF	FFF
D	FFF	FFF
E	E	FFF
F	FFF	FFF

Key:

= ROOT node

= AS0 node

= AS1 node

Tests Carried Out

- Periodic RAM scrubbing over an address range of 256 Kbytes
- Cyclic Redundancy Check (CRC) using the CCITT algorithm

Tools Used

ERC32

- AdaWorld-ERC32 X-Compilation System
- ERC32 SIS
- ERC32 Target Simulator from Spacebel

1750

- Ada-1750 X-Compiler (TLDada)
- 1750 Assembler (TLDasm)
- 1750 Linker (TLDlnk)
- MS1750 Simulator (ms1750)
- Ada Symbolic Debugger (TLDdbg)
- Environment Simulator (TLDenv) running the DPE HW Simulator developed by GMV for the INTEGRAL programme which provides improved timing accuracy.

Test Measurement Results

Target	Simulator	CRC-CCITT				RAM Scrubbing			
		Time (msecs)	Instruction Count	Cycle Count	CPI	Time (msecs)	Instruction Count	Cycle Count	CPI
1750A	TLDenv	18.89	21852	-	-	970.31	1442207	-	-
ERC32	SIS (ESTEC)	4.36	28432	43639	1.53	243.24	1446600	2432449	1.68
	Target Simulator (Spacebel)	7.45	50605	74524	1.47	246.30	1468422	2463007	1.68

Conclusions

- The 1750 suffers the overhead of the time-consuming XIO instructions required to read and modify the contents of the MMU page registers.
- If a programme needing >64Kwords RAM is targetted for a 1750, life is more difficult for the designer, implementors and test team than if the target were an ERC32.