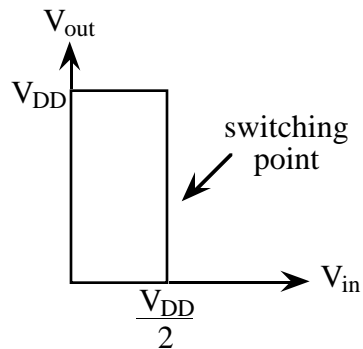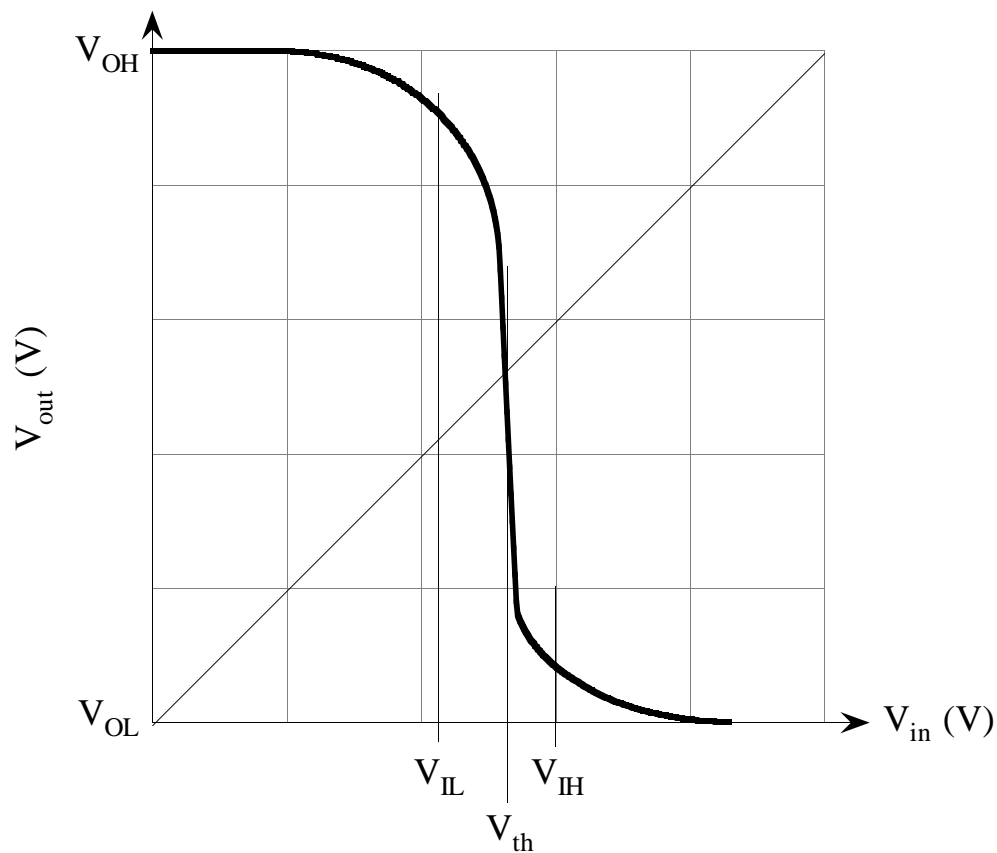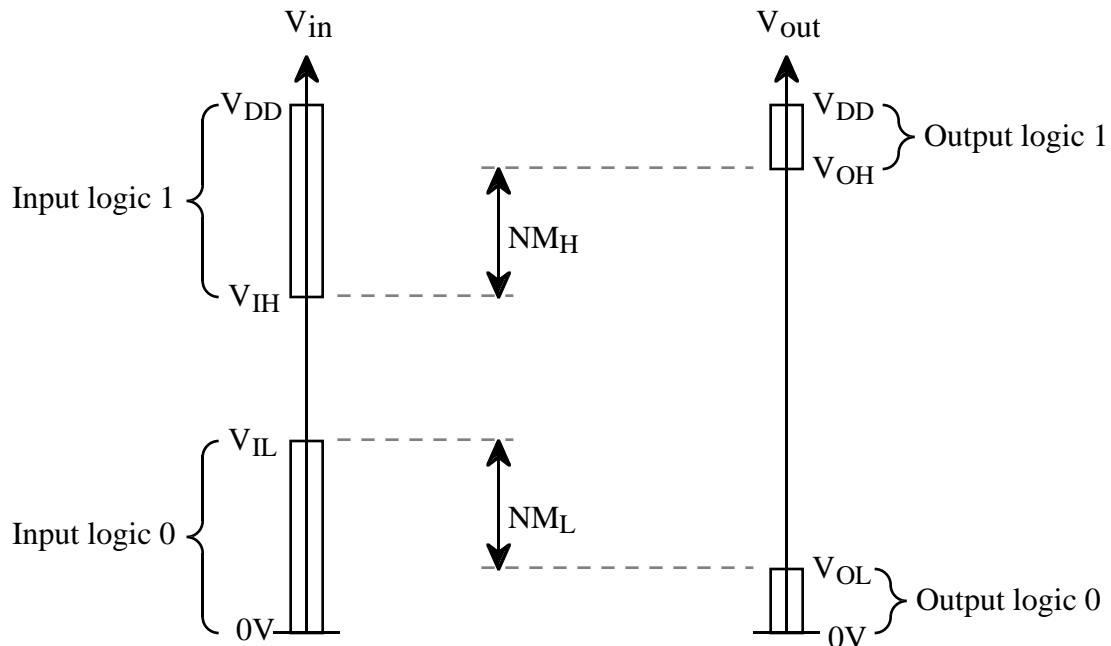# Ideal Inverter



# Actual Inverter Characteristics, some definitions



- $V_{IL}$ represents the maximum logic 0 (LOW) input voltage that will guarantee a logic 1 (HIGH) at the output

- $V_{IH}$ represents the minimum logic 1 (HIGH) input voltage that will guarantee a logic 0 (LOW) at the output

# Noise Margin

Illustration of Noise Margin:
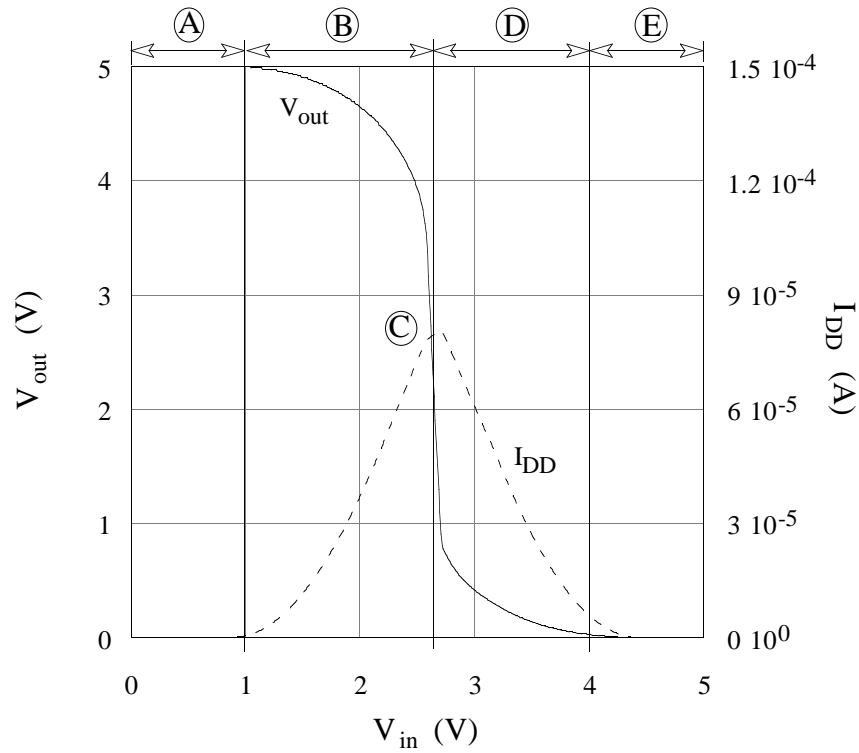


*Calculate* noise margin using

$$NM_L = V_{IL} - V_{OL} \qquad\qquad NM_H = V_{OH} - V_{IH}$$

How do we determine $V_{IL}$, $V_{OL}$, $V_{OH}$, and $V_{IH}$?

We must exam the inverter's transfer characteristic.

# CMOS Inverter Regions of Operation



Region A:

$0 \leq V_{in} < V_{Tn}$     $\Rightarrow$     $p$MOS nonsaturated (cutoff); $n$MOS cutoff

- $n$MOS is cutoff because $V_{in} < V_{Tn}$

Why is the $p$MOS device in the linear region?

Linear region $\equiv$ $V_{SDp} < V_{SGp} - |V_{Tp}|$

$$(5-5)V < (5-0)V - |-0.7|V$$
$$\text{[for } V_{DD} = 5V \text{ and } V_{Tp} = -0.7V]$$
$$0V < 4.3V$$

Note that the $p$MOS device can be in linear region even if $I_{Dp} \approx 0A$!

Region B:

$V_{Tn} \leq V_{in} < V_{th}$          $\Rightarrow$     $p$MOS nonsaturated, $n$MOS saturated

Why is $n$MOS saturated?          Is $V_{DSn} > V_{GSn} - V_{Tn}$?

Because $(V_{DSn} = V_{out}) > V_{th}$ and $(V_{GSn} = V_{in}) < V_{th}$ ,

then          $V_{DSn} > V_{GSn} - V_{Tn}$
              $V_{out} > V_{in} - V_{Tn}$                                   [B-1]

Why is $p$MOS in linear region?

It started out in linear and will remain in linear as long as

$$V_{SDp} < V_{SGp} - |V_{Tp}|$$
$$(V_{DD} - V_{out}) < (V_{DD} - V_{in}) - |V_{Tp}|$$
$$V_{in} < V_{out} - |V_{Tp}|  \qquad\qquad\qquad\text{[B-2]}$$

$V_{out}$ in the above expression (Eqn. [B-2]) is decreasing towards $V_{th}$ and $V_{in}$ is increasing towards $V_{th}$ . When Eqn. [B-2] no longer holds, then the $p$MOS device will become saturated.

For the $p$MOS device, then

regions A $\Rightarrow$ B $\Rightarrow$ C correspond to

linear $\Rightarrow$ linear $\Rightarrow$ saturated, respectively.

How can you predict the output voltage for region B?

The $n$MOS is saturated, so $I_{Dn} = \dfrac{\text{ß}_n}{2}\left(V_{in} - V_{Tn}\right)^2 = \dfrac{\text{ß}_n}{2}\left(V_{GSn} - V_{Tn}\right)^2$

The $p$MOS is linear, so

$$I_{Dp} = \frac{\text{ß}_p}{2}\left(2(V_{SGp} - |V_{Tp}|)V_{SDp} - (V_{SDp})^2\right)$$
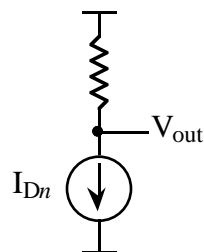
$$I_{Dp} = \frac{\text{ß}_p}{2}\left(2(V_{DD} - V_{in} - |V_{Tp}|)(V_{DD} - V_{out}) - (V_{DD} - V_{out})^2\right)$$

Can solve for $V_{out}$ since

$$I_{Dn} = I_{Dp}$$
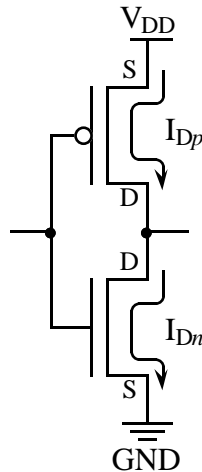


Equivalent circuit for region B $\Rightarrow$

Region C:

$V_{in} = V_{th}$          $\Rightarrow$   $p$MOS saturated, $n$MOS saturated

In order for $n$MOS to be saturated, need

$$V_{DSn} > V_{GSn} - V_{Tn}$$

$$V_{out} > V_{in} - V_{Tn}$$

In order for $p$MOS to be saturated, need

$$V_{SDp} > V_{SGp} - |V_{Tp}|$$

$$V_{DD} - V_{out} > V_{DD} - V_{in} - |V_{Tp}|$$
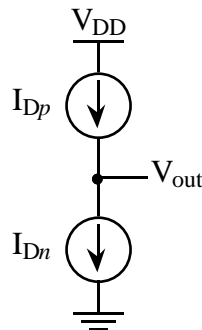
$$V_{out} < V_{in} + |V_{Tp}|$$

So $V_{out}$ in region C,

$$V_{in} - V_{Tn} < V_{out} < V_{in} + |V_{Tp}|$$

The CMOS inverter has very high gain in region C so small changes in $V_{in}$ produce large changes in $V_{out}$.  No closed form equation for $V_{out}$. Somewhere in this region, $V_{out} = V_{in}$, which is the switching point for this gate.

Equivalent circuit for region C:

What is $V_{in}$ in region C?

In region C, both devices in saturation so

$$I_{Dp} = \frac{\text{ß}_p}{2} (V_{DD} - V_{in} - |V_{Tp}|)^2$$

$$I_{Dn} = \frac{\text{ß}_n}{2} (V_{in} - V_{Tn})^2$$

So, using $I_{Dn} = I_{Dp}$, $V_{in}$ can be solved for (more on this later....)

Region D:

$V_{th} < V_{in} \leq V_{DD} - |V_{Tp}| \Rightarrow p$MOS saturated, $n$MOS linear

Hence,          $$I_{Dp} = \frac{\text{ß}_p}{2} (V_{DD} - V_{in} - |V_{Tp}|)^2$$

$$I_{Dn} = \frac{\text{ß}_n}{2} \left( 2(V_{in} - V_{Tn})V_{out} - V_{out}^2 \right)$$

Again, since $I_{Dp} = I_{Dn}$, we can solve for $V_{out}$:

$$V_{out}^2 - 2(V_{in} - V_{Tn})V_{out} + \frac{\text{ß}_p}{\text{ß}_n} (V_{DD} - V_{in} - |V_{Tp}|)^2 = 0$$

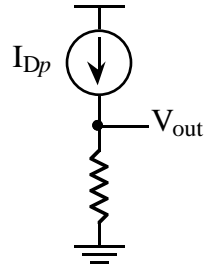using          $$x = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$$

and, recognizing from above,

$$a = 1, \, b = -2(V_{in} - V_{Tn}), \, c = \frac{\text{ß}_p}{\text{ß}_n} (V_{DD} - V_{in} - |V_{Tp}|)^2$$

we get

$$V_{out} = (V_{in} - V_{Tn}) - \sqrt{(V_{in} - V_{Tn})^2 - \frac{\beta_p}{\beta_n}(V_{in} - V_{DD} - |V_{Tp}|)^2}.$$

Equivalent circuit for region D $\Rightarrow$



Region E:

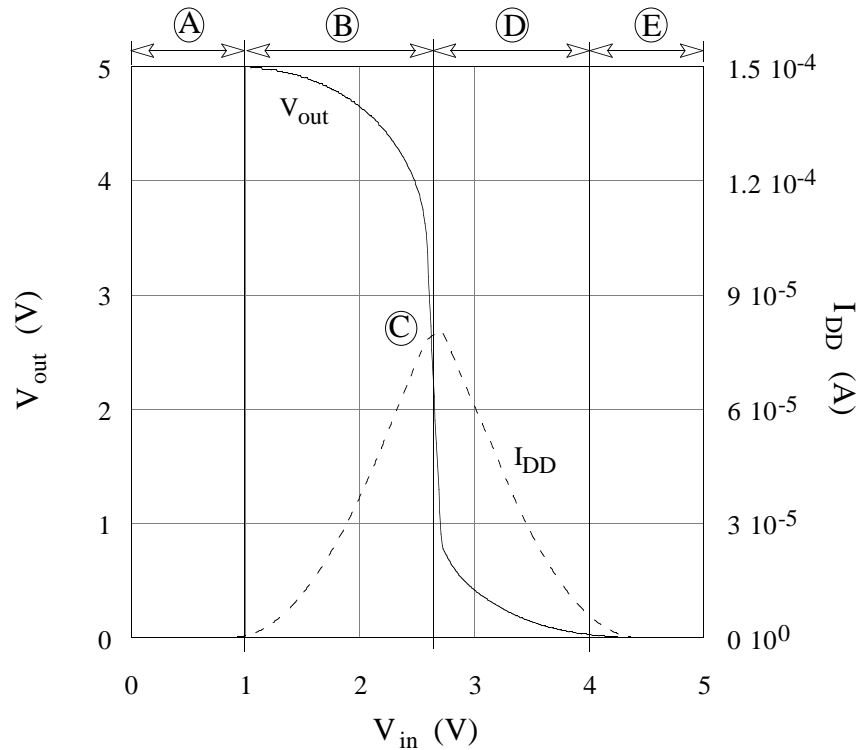$V_{in} > V_{DD} - |V_{Tp}|$          $\Rightarrow$          $p$MOS is cutoff, $n$MOS is linear mode

Since $V_{SGp} = V_{DD} - V_{in}$ ($< |V_{Tp}|$),

$$\therefore V_{out} \approx 0V$$

due to $n$MOS acting as pull-down while $p$MOS in cutoff.

# CMOS Inverter Transfer Characteristic



Analysis:

$V_{OH}$:   $V_{in} < V_{Tn}$, the $n$MOS transistor is in cutoff while the $p$MOS transistor is turned-on (inversion layer established).  The result is

$$V_{OH} \approx V_{DD} \, .$$

$V_{OL}$:   $(V_{DD} - V_{in}) < |V_{Tp}|$, the $p$MOS is in cutoff while the $n$MOS is on and providing a conduction channel to ground.  Hence,

$$V_{OL} \approx 0V.$$

$V_{IL}$:   Input low voltage, here the $n$MOS transistor is saturated and the $p$MOS is nonsaturated.  Equating the currents provides

$$\frac{\text{ß}_n}{2} (V_{IL} - V_{Tn})^2 =$$

$$\frac{\text{ß}_p}{2} \Big( 2(V_{DD} - V_{IL} - |V_{Tp}|)(V_{DD} - V_{out}) - (V_{DD} - V_{out})^2 \Big).$$

$V_{IL}$:   (continued)   Since two unknowns exist, $V_{in} = V_{IL}$ and $V_{out}$, a second equation is needed.   Use the unity-gain condition to obtain this second equation,

$$\frac{dV_{out}}{dV_{in}} = \frac{(\partial I_{Dn}/\partial V_{in}) - (\partial I_{Dp}/\partial V_{in})}{(\partial I_{Dp}/\partial V_{out})} = -1,$$

provides

$$V_{IL}\left(1 + \frac{\beta_n}{\beta_p}\right) = 2V_{out} + \frac{\beta_n}{\beta_p} V_{Tn} - V_{DD} - |V_{Tp}| \ .$$

Now the two equations needed to solve for $V_{IL}$ and $V_{out}$ exist.

$V_{IH}$:   Input high voltage, here the $n$MOS is nonsaturated and the $p$MOS is saturated.   Equating the drain currents yields

$$\frac{\beta_n}{2}\left(2(V_{IH} - V_{Tn})V_{out} - V_{out}^2\right) = \frac{\beta_p}{2} (V_{DD} - V_{IH} - |V_{Tp}|^2),$$

the first of two equations needed to solve two unknowns, $V_{in} = V_{IH}$ and $V_{out}$.   Use the unity-gain condition to get the second,

$$\frac{dV_{out}}{dV_{in}} = \frac{(\partial I_{Dp}/\partial V_{in}) - (\partial I_{Dn}/\partial V_{in})}{(\partial I_{Dn}/\partial V_{out})} = -1.$$

This provides

$$V_{IH}\left(1 + \frac{\beta_p}{\beta_n}\right) = 2V_{out} + V_{Tn} + \frac{\beta_p}{\beta_n} (V_{DD} - |V_{Tp}|) \ ,$$

the second equation needed to solve for the two unknowns.

$\mathbf{V}_{th}$:   At the CMOS inverter's switching point, or *inverter threshold*, $V_{th} = V_{in} = V_{out}$ and both the *p*MOS and *n*MOS transistors are saturated. Again, equating the drain currents,

$$\frac{\text{ß}_n}{2} (V_{th} - V_{Tn})^2 = \frac{\text{ß}_p}{2} (V_{DD} - V_{th} - |V_{Tp}|)^2$$

is obtained which can be easily solved to provide $V_{th}$,

$$V_{th} = \frac{V_{Tn} + \sqrt{\frac{\text{ß}_p}{\text{ß}_n}} (V_{DD} - |V_{Tp}|)}{\left(1 + \sqrt{\frac{\text{ß}_p}{\text{ß}_n}}\right)} \, .$$

**Note**: switching point of gate ($V_{th}$) is $\dfrac{V_{DD}}{2}$ -*if*- $\dfrac{\text{ß}_n}{\text{ß}_p} = 1$ and $V_{Tn} = -V_{Tp}$.

So, switching point of inverter is function of the ratio of the *n*MOS/*p*MOS gains and the threshold voltages of the *n*MOS, *p*MOS transistors.

# ß$_n$ / ß$_p$  Ratio

The ß$_n$ (gain of $n$MOS) / ß$_p$ (gain of $p$MOS) ratio determines the switching point of the CMOS inverter.
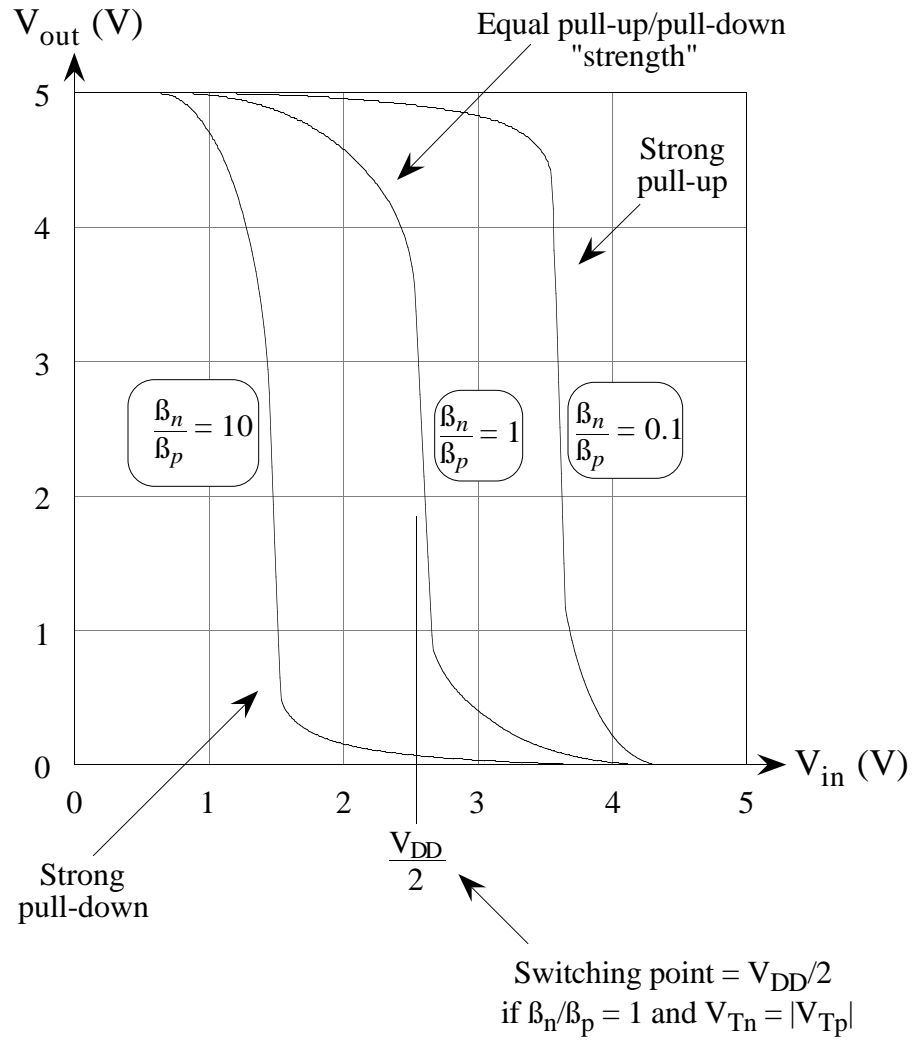
Recall that

$$\text{ß} = \frac{\mu\varepsilon}{t_{ox}} \frac{W}{L} \ .$$

If we assume that the *n*MOS and *p*MOS transistors have equal W/L ratios, then

$$\frac{\text{ß}_n}{\text{ß}_p} = \frac{\dfrac{\mu_n\varepsilon}{t_{ox}} \dfrac{W_n}{L_n}}{\dfrac{\mu_p\varepsilon}{t_{ox}} \dfrac{W_p}{L_p}} = \frac{\mu_n}{\mu_p} = \frac{\text{electron mobility}}{\text{hole mobility}} \ .$$

In <u>silicon</u>, the ratio $\mu_n/\mu_p$ is usually between 2 to 3.

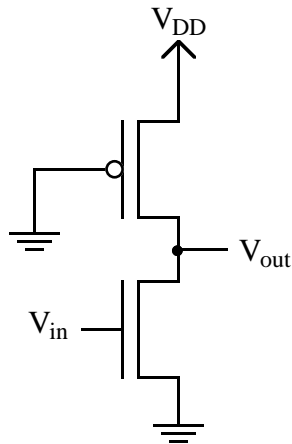This means, that if                      $L_n = L_p,$

then                      $W_p$ must be 2 to 3 times $W_n$

in  order  for                      $\text{ß}_n = \text{ß}_p$ .

if $\dfrac{W_p}{L_p} = \dfrac{W_n}{L_n}$ because $\dfrac{\text{ß}_n}{\text{ß}_p} > 1$
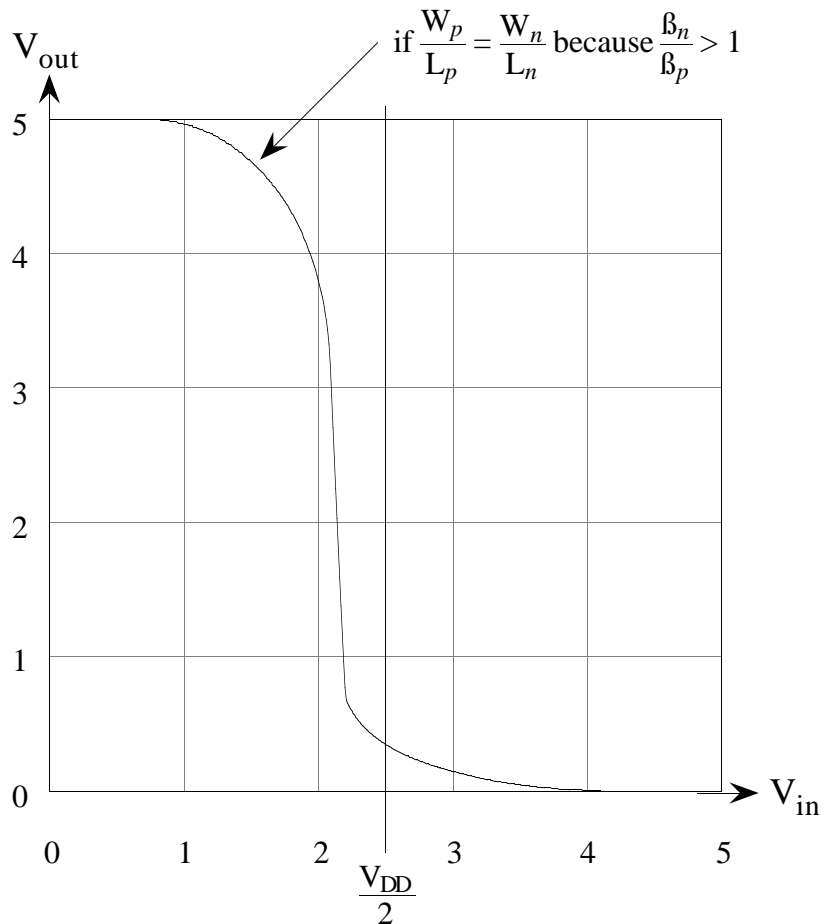
Calculate the switching point of a static load inverter as function of $\beta_n/\beta_p$:

In region C, already know *n*MOS device is saturated from previous analysis.

For *p*MOS to be saturated need:

$$V_{SDp} > V_{SGp} - |V_{Tp}|$$
$$V_{DD} - V_{out} > V_{DD} - 0V - |V_{Tp}|$$
$$V_{out} < |V_{Tp}|$$
Not true!!!
(If $V_{out}$ in region C is about $\f(V_{DD},2)$
and $\dfrac{V_{DD}}{2} > |V_{Tp}|$
(typically this is true))

$\therefore$ *p*MOS must be in linear region

Then
$$I_{Dn} = \frac{\beta_n}{2}(V_{GSn} - V_{Tn})^2 = \frac{\beta_n}{2}(V_{in} - V_{Tn})^2$$

and
$$I_{Dp} = \frac{\beta_p}{2}\left(2(V_{SGp} - |V_{Tp}|)V_{SDp} - V_{SDp}^{2}\right)$$

$$I_{Dp} = \frac{\beta_p}{2}\left(2(V_{DD} - |V_{Tp}|)(V_{DD} - V_{out}) - (V_{DD} - V_{out})^2\right)$$

Equate $I_{Dn} = I_{Dp}$ and solve for $V_{out}$.

$$V_{out} = |V_{Tp}| + \sqrt{(V_{DD} - |V_{Tp}|)^2 - \frac{\beta_n}{\beta_p}(V_{in} - V_{Tn})^2}$$

Can also solve for $\beta_n/\beta_p$,

$$\frac{\beta_n}{\beta_p} = \frac{(V_{DD} - |V_{Tp}|)^2 - (V_{out} - |V_{Tp}|)^2}{(V_{in} - V_{Tn})^2}$$

Consider again

$$\frac{\text{ß}_n}{\text{ß}_p} = \frac{(V_{DD} - |V_{Tp}|)^2 - (V_{out} - |V_{Tp}|)^2}{(V_{in} - V_{Tn})^2}$$

for the pseudo-$n$MOS inverter.

Let $|V_{Tp}| = V_{Tn} = 0.2V_{DD}$ and $V_{in} = V_{out} = \dfrac{V_{DD}}{2}$. Then, for $V_{DD} = 5V$,

$$\frac{\text{ß}_n}{\text{ß}_p} \approx 6.1 \ !!!$$

Note that this is *very* different result from the CMOS inverter case!

If $V_{DD} = 3.3V$, but the value of $V_{Tn} = |V_{Tp}|$ is unchanged (i.e., 1V in the above example), then

$$\frac{\text{ß}_n}{\text{ß}_p} \approx 11.5$$

for a switching point equal to $\dfrac{V_{DD}}{2}$.

The $\text{ß}_n/\text{ß}_p$ ratio depends on the absolute value of $V_{DD}$! This means that the operation of the pseudo-$n$MOS inverter will NOT scale with $V_{DD}$ (for a given CMOS technology).

For the CMOS inverter, the $\text{ß}_n/\text{ß}_p$ ratio for a switching point of $V_{DD}/2$ is *independent* of $V_{DD}$ so its operation <u>will</u> <u>scale</u> with supply voltage. This is a another big advantage of CMOS technology.

Not unusual for static CMOS circuits to operate over a <u>very</u> <u>large</u> range of power supply voltages, i.e., 2.0V to 6.0V is common.