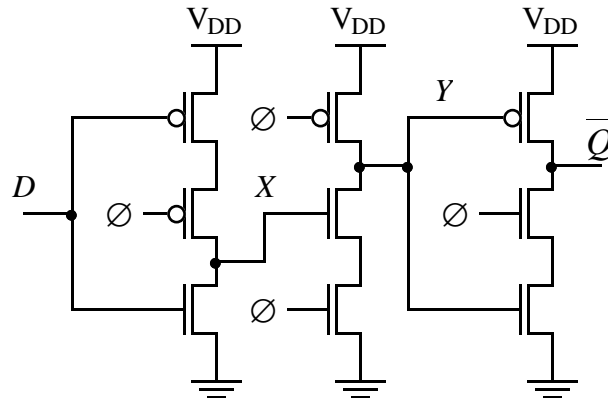


## Observations for other Positive Edge-Triggered D-FF

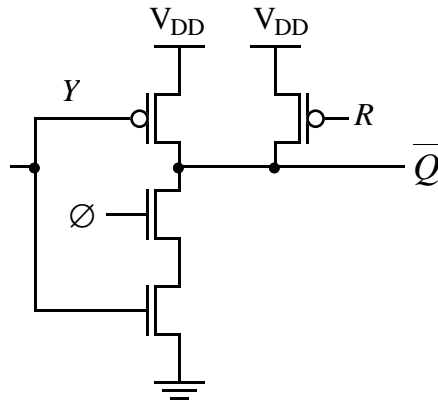


positive edge-triggered TSPC D-flip flop (non-split output)

Need to analyze for clock = 0 (master sampling, slave holding), clock 0 → 1, clock = 1:

clock	D	X	Y	$\bar{Q}$
0	0	1	1	$\bar{Q}_{old}$
0	1	0	1	$\bar{Q}_{old}$

Need to force  $\bar{Q}_{old}$  to a "1". Can do it by → → → → → → → → →

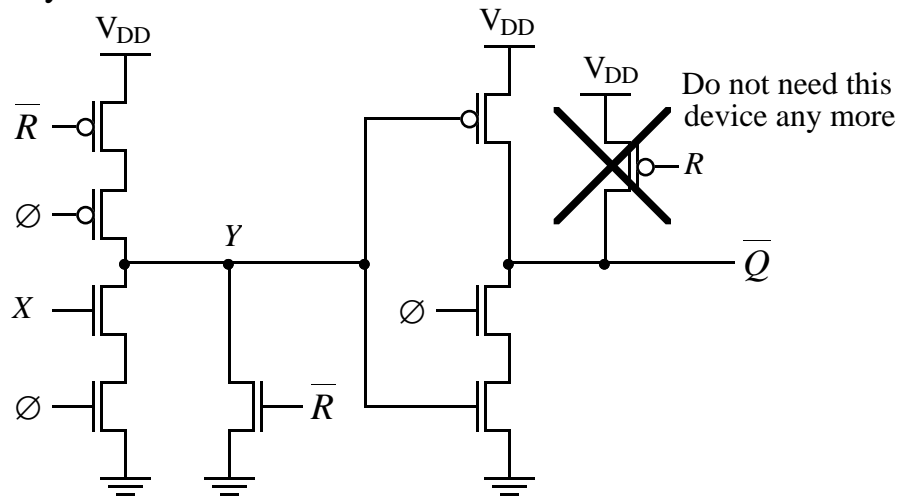


Check other cases:

clock	D	X	Y	$\bar{Q}$
0 → 1	0	$X_{old} (= 1)$	0	1
0 → 1	1	$X_{old} (= 0)$	$Y_{old} (= 1)$	0

For the above case where clock is going 0 → 1 and D = 0, no reset is needed. In the second case above where clock is going 0 → 1 and D = 1, we need to force  $Y_{old}$  to be a zero when reset is asserted. How to do this?

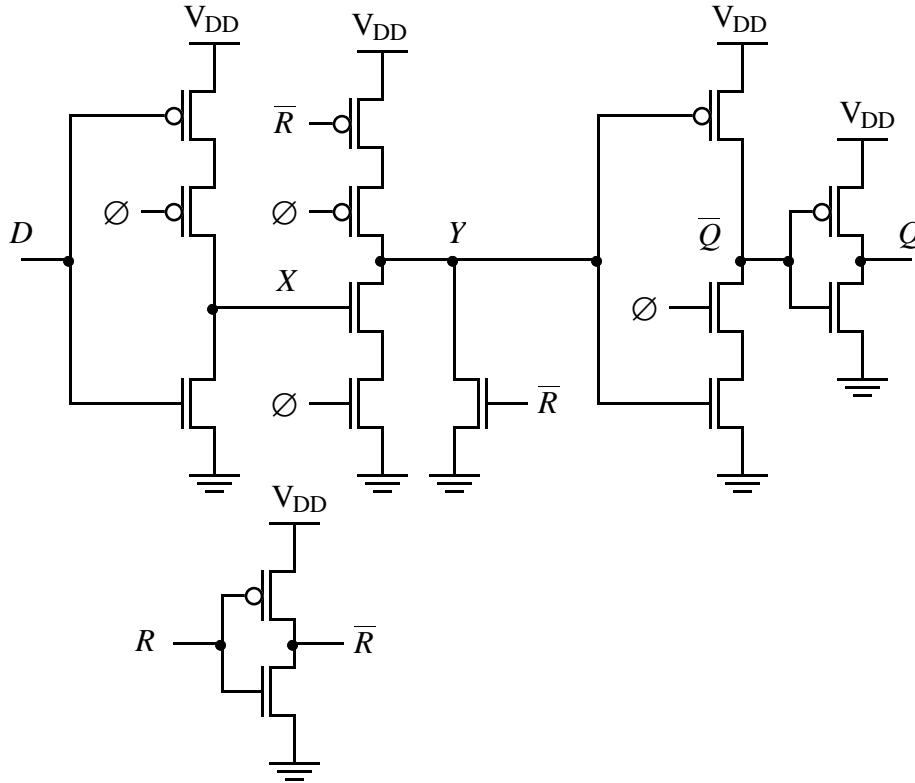
Here's one way:



When clock ( $\emptyset$ ) = 0  $\rightarrow$  1,  $R = 0$ ,  $\bar{R} = 1$ , then forces  $Y$  node = 0. Even works when clock = 0, can get rid of pMOS pullup on  $\bar{Q}$  output.

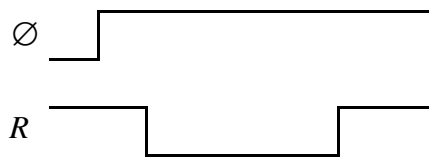
Will have to invert  $R$  inside of circuit because  $R$  is low true, so final transistor count for adding asynchronous low true reset is 4.

Final circuit (positive edge-triggered TSPC *D*-flip flop with asynchronous, low-true reset):

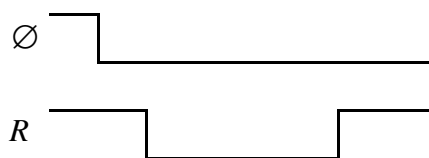


Final transistor count = 15. Recall again that a static *D*-flip flop can require 33 transistors!

Final check →



$$\begin{aligned} X &= X_{old} & Y &= Y_{old} \\ Y &= 0 & \bar{Q} &= 1 \\ \bar{Q} &= 1 \end{aligned}$$



$$\begin{aligned} X &= \overline{\text{data}} & Y &= 1 \\ Y &= 0 & \bar{Q} &= \bar{Q}_{old} = 1 \\ \bar{Q} &= 1 \end{aligned}$$