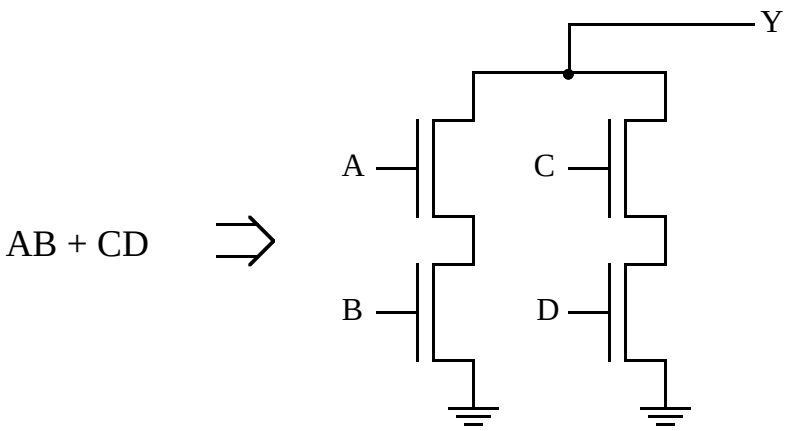
# More Complex Gates

$F = \overline{AB + CD} \quad \Rightarrow \quad N_{tree}$ will provide 0's, $P_{tree}$ will provide 1's

0's of function F is $\overline{F}$, $\Rightarrow$ $\overline{F} = \overline{\overline{AB + CD}} = AB + CD$

*n*MOS transistors need high true inputs, so it is desirable for all input variables to be high true, just as above.



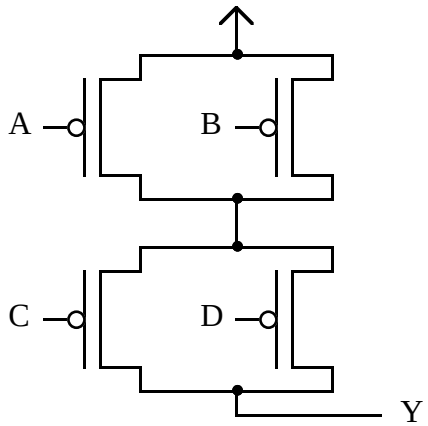

Likewise, a $P_{tree}$ will provide 1's.

$F = \overline{AB + CD}$, need a form involving $\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{D}$

Apply DeMorgan's Theorem:

$F = \overline{AB} \cdot \overline{CD} = (\overline{A} + \overline{B}) \cdot (\overline{C} + \overline{D})$

Implementation $\Rightarrow$

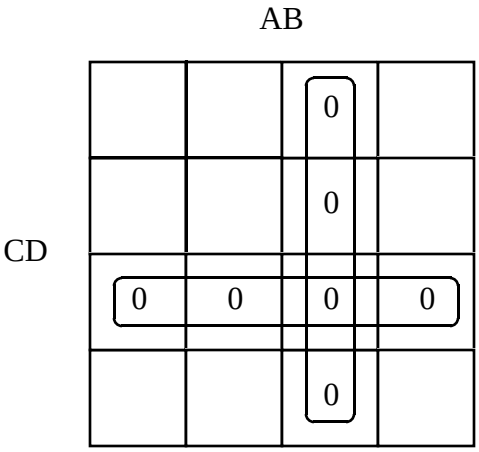


Can also use K-maps:

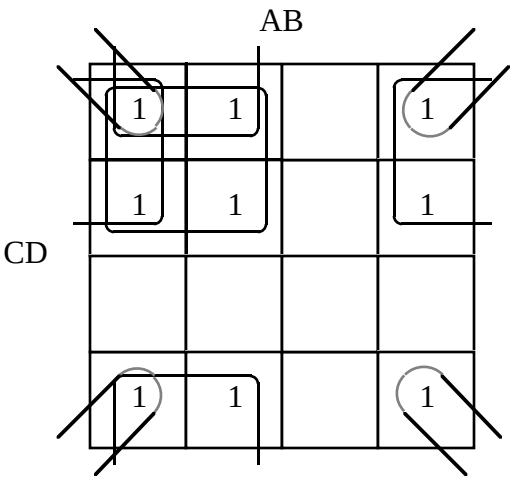
$$F = \overline{AB + CD}$$

| CD \ AB | | | | |
|---|---|---|---|---|
| | 1 | 1 | 0 | 1 |
| | 1 | 1 | 0 | 1 |
| | 0 | 0 | 0 | 0 |
| | 1 | 1 | 0 | 1 |

For $N_{tree}$, minimize 0's; for $P_{tree}$, minimize 1's

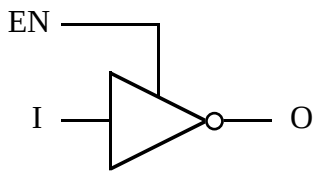



$$N_{tree} = AB + CD$$




$$P_{tree} = \overline{A}\cdot\overline{C} + \overline{A}\cdot\overline{D} + \overline{B}\cdot\overline{C} + \overline{B}\cdot\overline{D}$$
$$= \overline{A}\,(\overline{C} + \overline{D}) + \overline{B}\,(\overline{C} + \overline{D})$$
$$= (\overline{A} + \overline{B}) \cdot (\overline{C} + \overline{D})$$

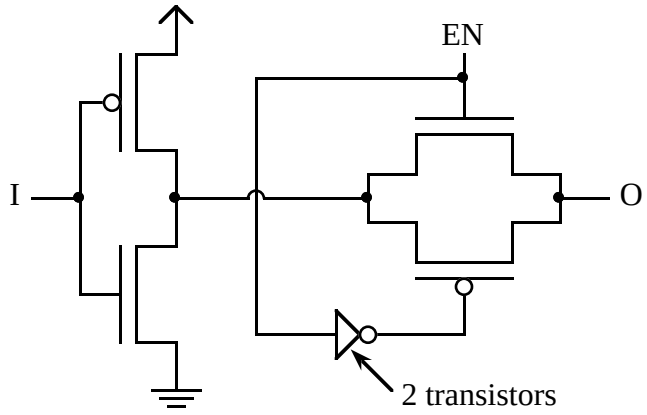
# Tri State Inverter




| EN | I | O |
|---|---|---|
| 0 | X | Z |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

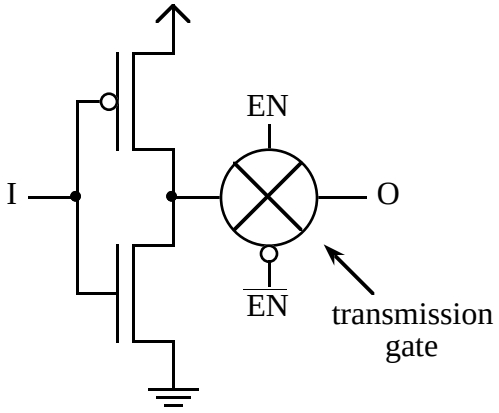
"Z" is high impedance state

Implementation? Here is one method:

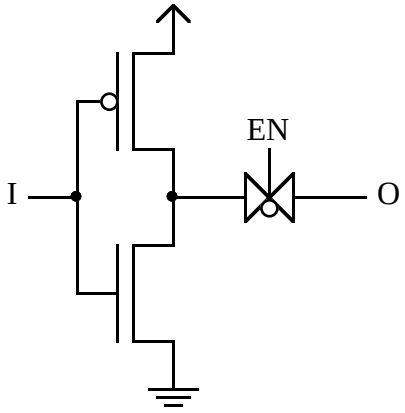



6 transistors total

Alternate representations:

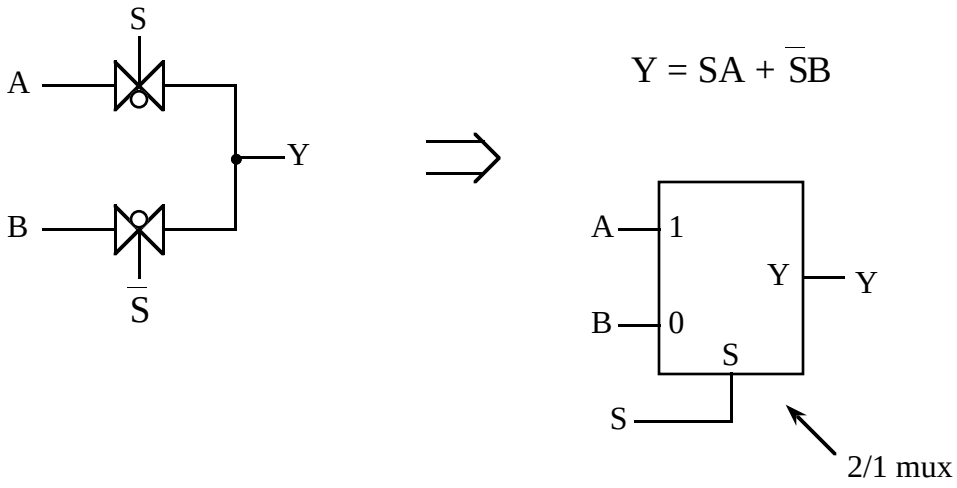



or




where the connection for $\overline{EN}$ is *understood* or *implied*, $\overline{EN}$ still needs to somehow be provided in the physical circuit

# Transmission Pass Gate Logic



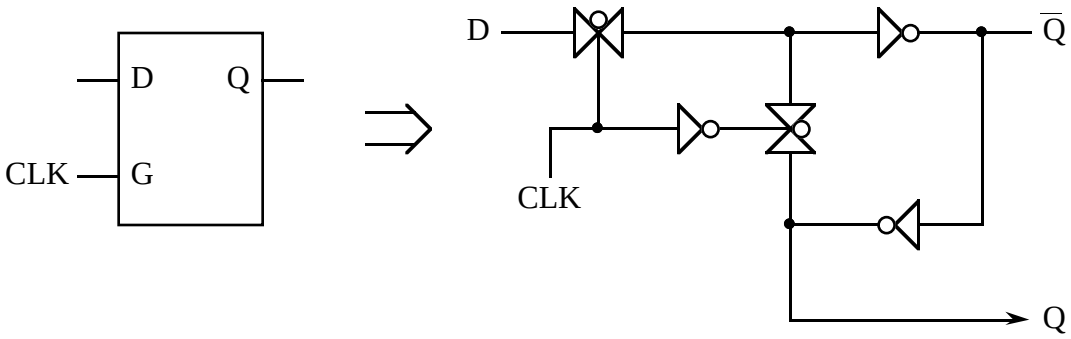

Will require

(4 transistors for two pass gates) + (2 transistors for inversion of S)

= 6 transistors total

This technique uses less transistors than a design using normal gates, but is <u>non-restoring</u>. Pass gate logic has no drive capability. Drive comes from orginal A, B inputs.

A D-Latch using transmission gates:



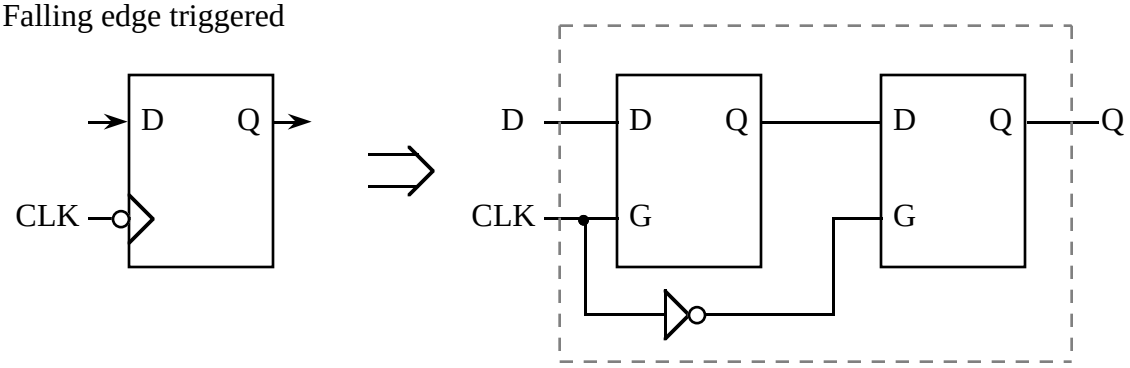

when CLK = 1, Q = D

CLK = 0, Q= $Q_{old}$

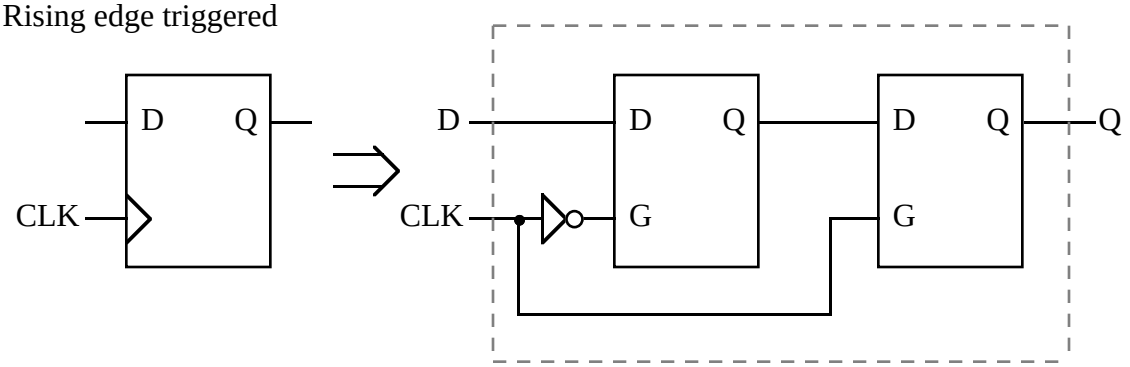
Recall flip-flop construction from CAD course (edge triggered device) —

→ two latches in a master-slave arrangement are required

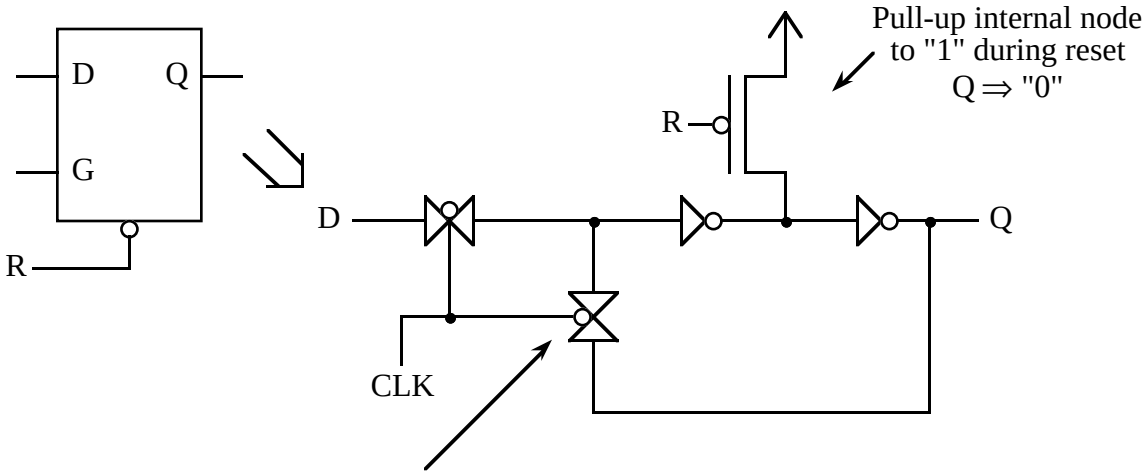
Falling edge triggered




Rising edge triggered

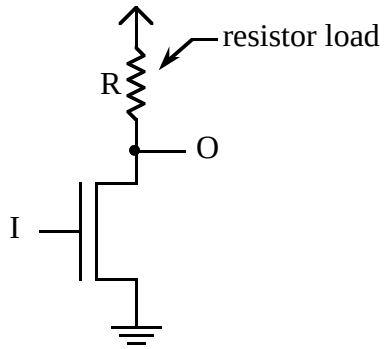



How would a D-Latch with an asynchronous reset be implemented?



# Introduction to Static Load Inverters

**1)**




When I = 1, inverter dissipates static power.

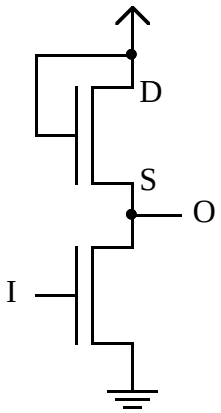
Switching point of inverter depends on ratio of R to $R_{ON}$ (on resistance of *n*MOS device.

$V_{OH}$ = 5V,

$V_{OL} \approx$ 0V, depends on ratio of $R/R_{on}$

Note: output can swing from 0V to 5V (Vdd)

**2)**




Load is enhancement-mode *n*MOS device.

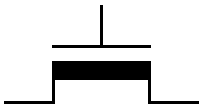
Again, static power dissipation occurs when I = 1.

Note: output swings from ≈0V to (Vdd - $V_{Tn}$)

Using a transistor as a load tends to require <u>much</u> <u>less</u> silicon area than a resistor.

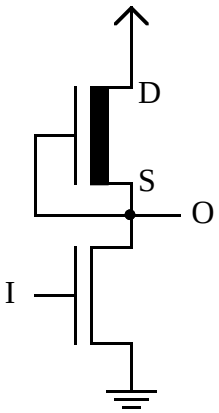
$V_{OH}$ = Vdd - $V_{Tn}$,
$V_{OL} \approx$ 0V, depending on ratio of $R_{ON}$ of two enhancement devices

Depletion-mode *n*MOS



*n*MOS device with $V_{Tn} < 0V$ (negative threshold voltage). Device is always conducting if $V_{GS} > 0V$.

**3 )**




$V_{GS} = 0V$ always

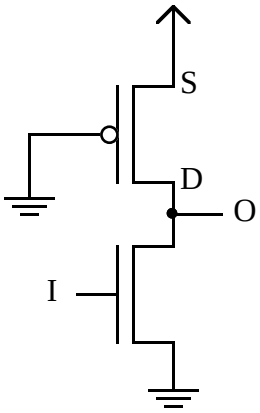
Load device is always on, looks like a load resistor.

Dissipates static power when I = 1

$V_{OH} = 5V$; $V_{OL} \approx 0V$, depending on ratio of $R_{ON,dep}$ to $R_{ON,enh}$.

Depletion-mode devices were used before it was economical to put both *p*-type and *n*-type devices on the same die.

**4)** *p*MOS device as static load

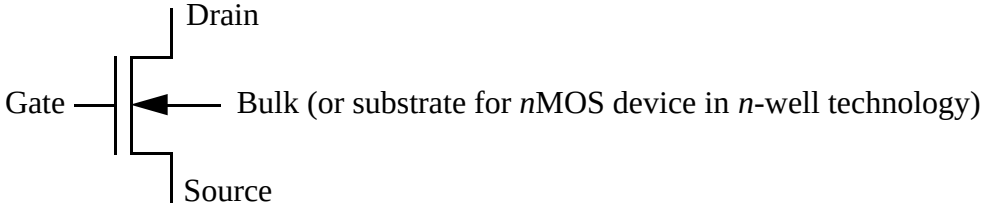



Here also the load device is <u>always</u> on (conducting).

Dissipates static power when I = 1.

$V_{OH} = 5V$; $V_{OL} \approx 0V$, depending on ratio of $R_{ON,p}$ to $R_{ON,n}$

# Basic MOS Device Equations




The *n*MOS device is a *four* terminal device: Gate, Drain, Source, Bulk.

Bulk (substrate) terminal is normally ignored at schematic level, usually tied to ground for the *n*MOS case. In analog applications, however, the bulk terminal may not be ignored.

Gate controls channel formation for conduction between Drain and Source. Drain at higher potential than Source — Source usually tied to GND to act as pull-down (*n*MOS).

Three regions of operations — first-order (*ideal*) equations:

Cutoff region

$I_D = 0A$ $\qquad V_{GS} \le V_{Tn}$ (*n*MOS threshold voltage)

Linear region

$$I_D = ß\left((V_{GS} - V_{Tn})V_{DS} - \frac{V_{DS}^2}{2}\right) \qquad 0 < V_{DS} < V_{GS} - V_{Tn}$$

Note: $I_D$ is linear with respect to $(V_{GS} - V_{Tn})$ only when $\frac{V_{DS}^2}{2}$ is small.

Saturation region

$$I_D = \frac{ß}{2}(V_{GS} - V_{Tn})^2 \qquad 0 < V_{GS} - V_{Tn} < V_{DS}$$

Device parameters:

ß = transistor gain factor, dependent on process parameters and device geometry

process dependent, constant

$$ß = \left(\frac{\mu\varepsilon}{t_{ox}}\right)\left(\frac{W}{L}\right)$$

under control of the designer

As W/L increases, effective $R_{ON}$ of device decreases

$\mu$ = surface mobility of the carriers in the channel

$\varepsilon$ = permittivity of the gate insulator

$t_{ox}$ = thickness of the gate insulator

See Figure 2.5, 2.8 concerning $\mu$, $\varepsilon$, and $t_{ox}$

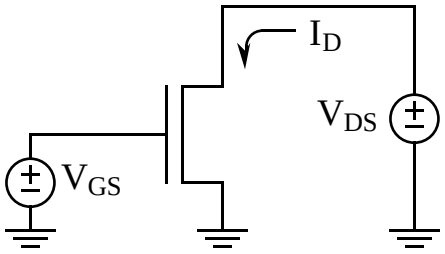
SPICE represents ß by a factor given by

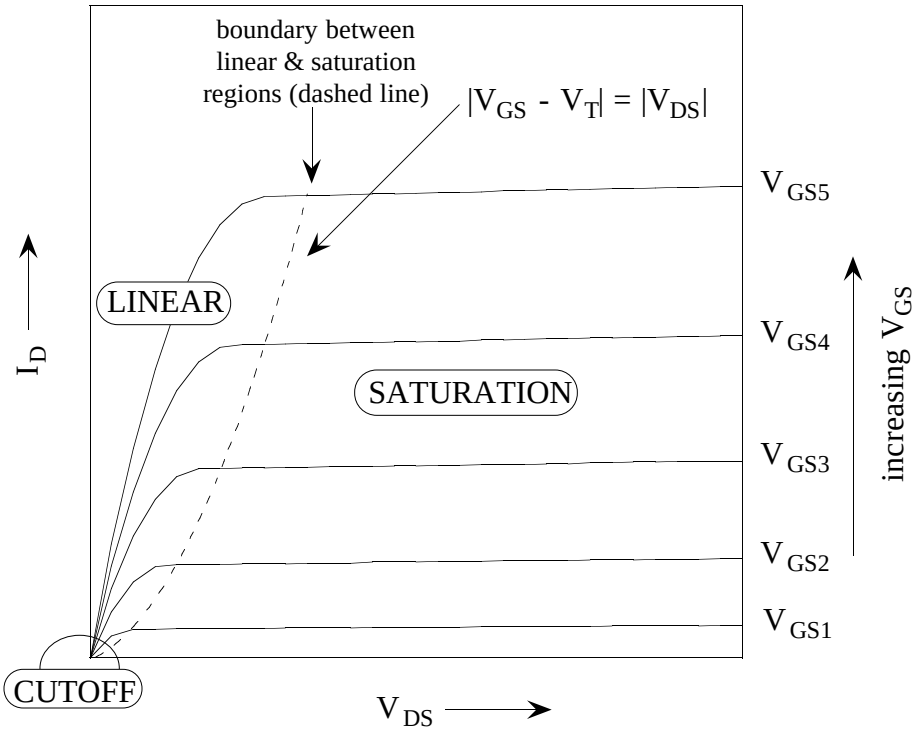
$$K' = \mu C_{ox} = \mu \frac{\varepsilon}{t_{ox}} = \mathbf{KP}$$

So,

$$I_D = \frac{K'}{2}\frac{W}{L}\left(V_{GS} - V_{Tn}\right)^2; \qquad \text{saturation region}$$

# VI characteristic




Things to note:

In the "linear" region, $I_D$ becomes less and less linear with $V_{GS}$ as $V_{DS}$ becomes large. This is because the $\frac{V_{DS}^2}{2}$ term in the linear region grows large.

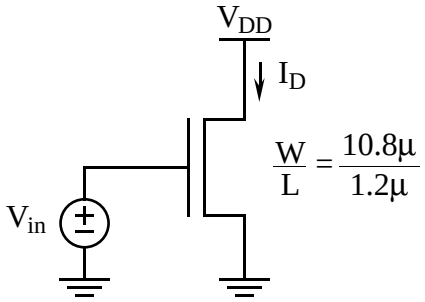
Higher $V_{GS}$ values increase channel conductance allowing for higher values of $I_D$ for a given $V_{DS}$.

## Predicting $I_D$ values with ideal equations

In saturation region,

$$I_D = K'\left(\frac{W}{L}\right)\frac{(V_{GS} - V_T)^2}{2}$$

If we have




then we can calculate $I_D$ based on $V_{in}$, K', $V_T$ (MOSFET parameters).

In specifying W, L values, these are often given in a <u>dimensionless</u> unit called <u>lambda</u>.

When mapping the transistor schematic/layout to a particular technology, the actual W, L will be calculated as:

W' (actual, microns (μ)) = W × lambda (microns)
L' (actual, microns) = L × lambda (microns)

So lambda is a scaling factor. Note that the ratio $\frac{W}{L}$ is what is important, and that

$$\frac{W'}{L'} = \frac{W \times \text{lambda}}{L \times \text{lambda}} = \frac{W}{L}\ .$$

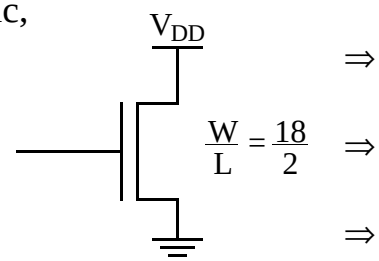
Scaling factor lambda allows transistor $\frac{W}{L}$ values specified in schematics to be technology independent.

For MOSIS foundry vendors,

2.0μ technology $\Rightarrow$ lambda = 1.0
1.2μ technology $\Rightarrow$ lambda = 0.6
0.8μ technology $\Rightarrow$ lambda = 0.4.

Note, however, that lambda *is not* always $\frac{1}{2}$ technology miniumum feature size (line width). Scaling factor lambda *is* foundry/silicon vendor dependent.

In schematic,




$\Rightarrow$

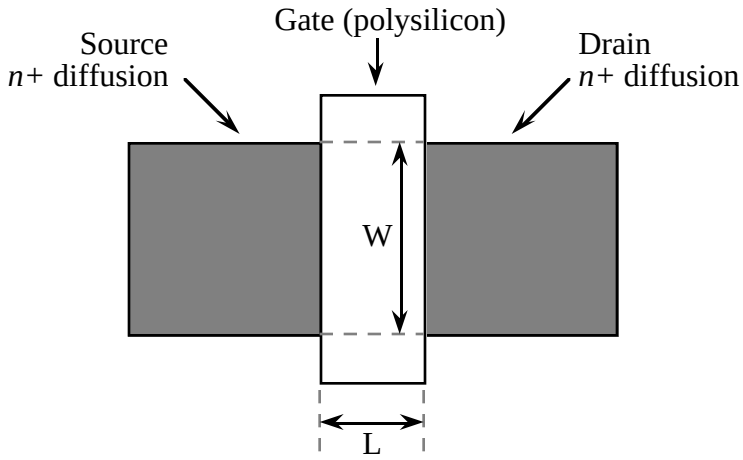
$\Rightarrow$

$\Rightarrow$

mapped to 1.2μ technology,

$$\frac{W}{L} = \frac{10.8\mu}{1.2\mu}$$

*n*MOSFET layout:



In digital logic, typically will draw all transistors with the minimum gate length (= 2 × lambda) and vary the width.

Larger W ⇒ larger transconductance (more current flow for given gate voltage), higher gate capacitance

During fabrication process, the actual width and length of the channel can be *reduced* by diffusion from the bulk, source, and drain into the device channel.

SPICE has some MOSFET model parameters to account for this effect, LD and WD, where the actual the actual length and width is calculated as

$$L_{effective} = L_{drawn} - 2 \times LD$$

$$W_{effective} = W_{drawn} - 2 \times WD$$

If LD, WD parameters not specified in the model, then SPICE assumes they are 0.