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How to Implement Digital IF

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School of Electronic Engineering

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Advanced Mobile Communication Systems Research Group

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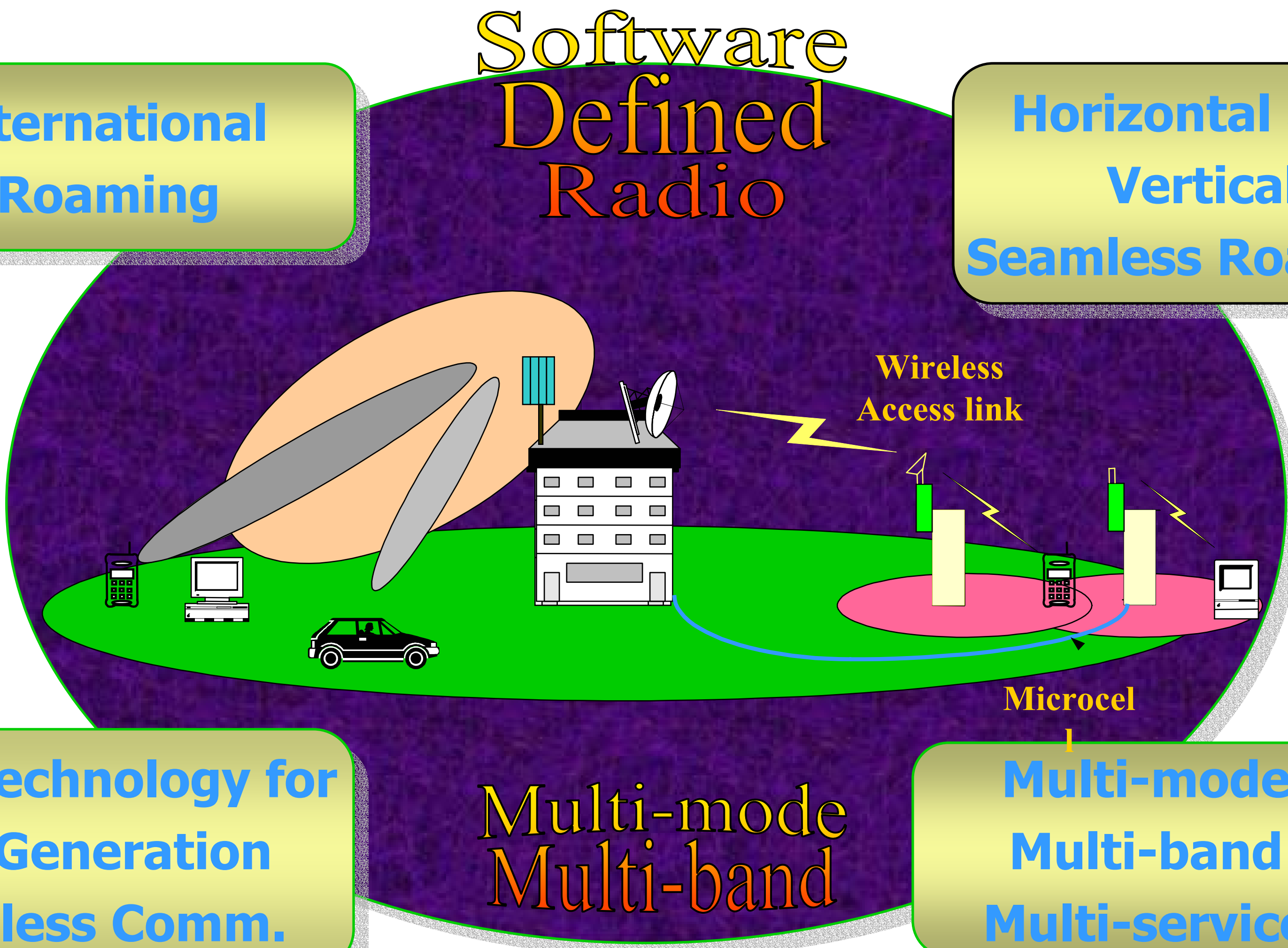
Contents

- Background
- SDR for beyond 3G
- What is Digital IF?
- ADC & DAC Technology for Digital IF
- Filtering Technology for Digital IF
- Digital IF based Channelization
- Conclusion

SDR for Beyond 3G

International Roaming

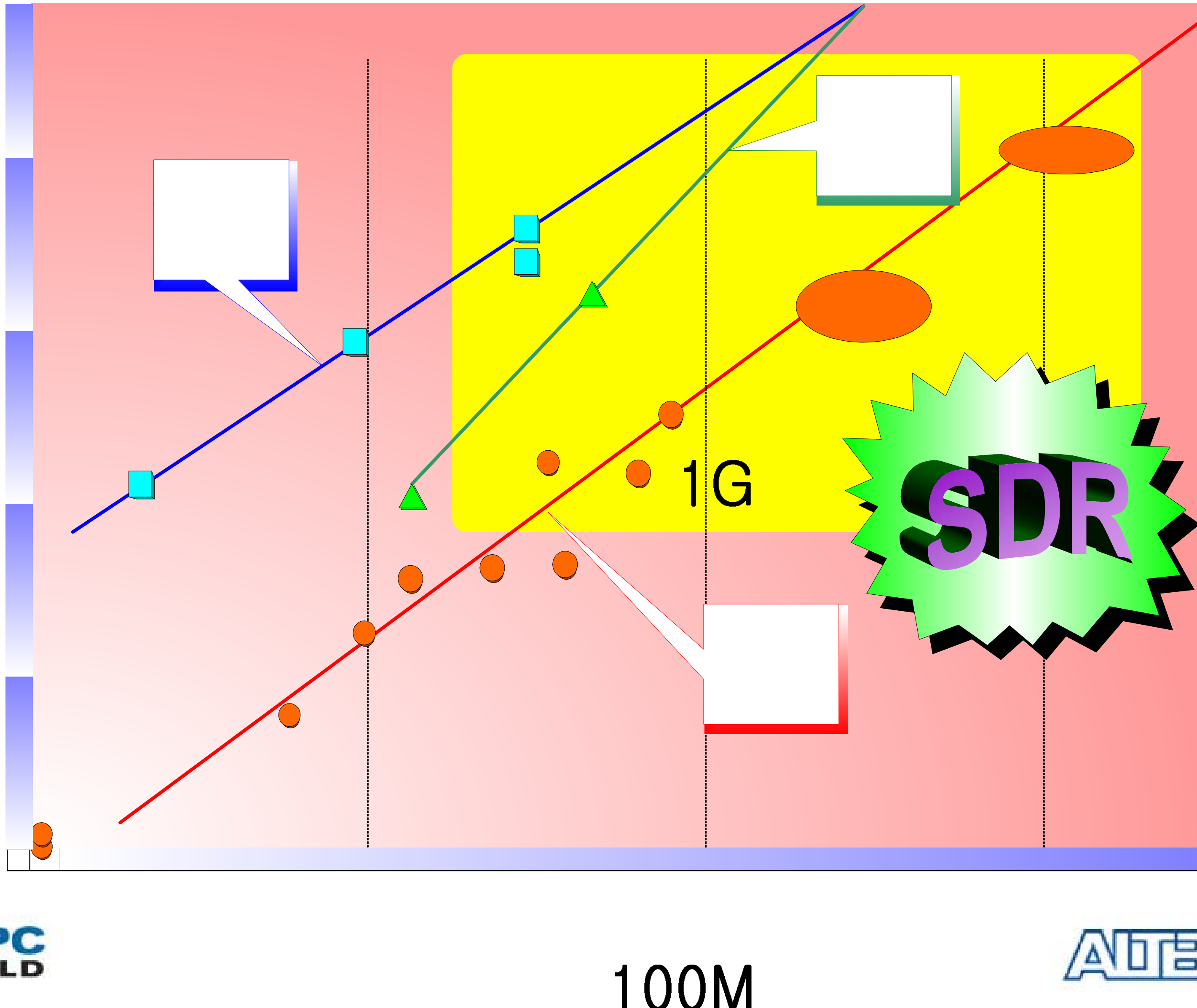
Horizontal and Vertical Seamless Roaming



Core Technology for 4^{th} Generation Wireless Comm.

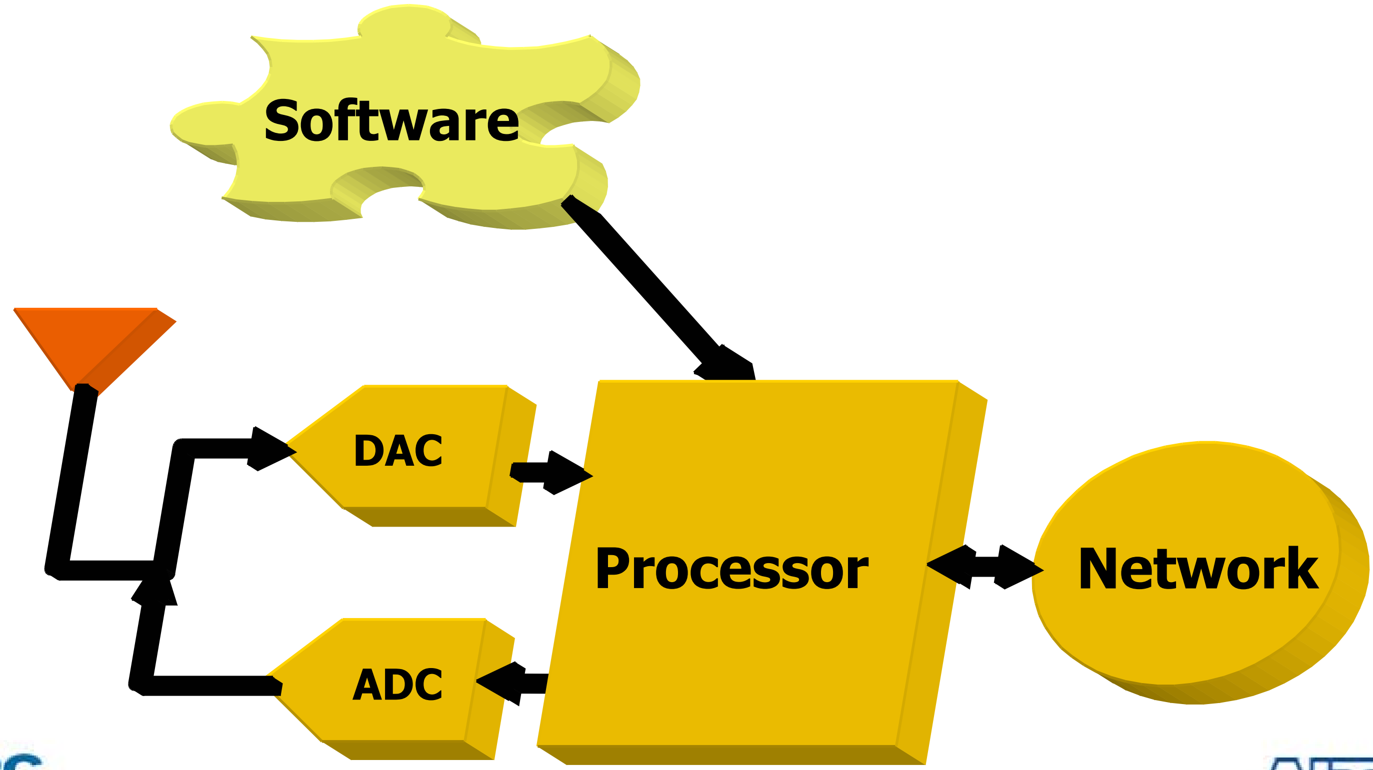
Multi-mode
Multi-band
Multi-service

Evolution of Wireless Comm. Systems

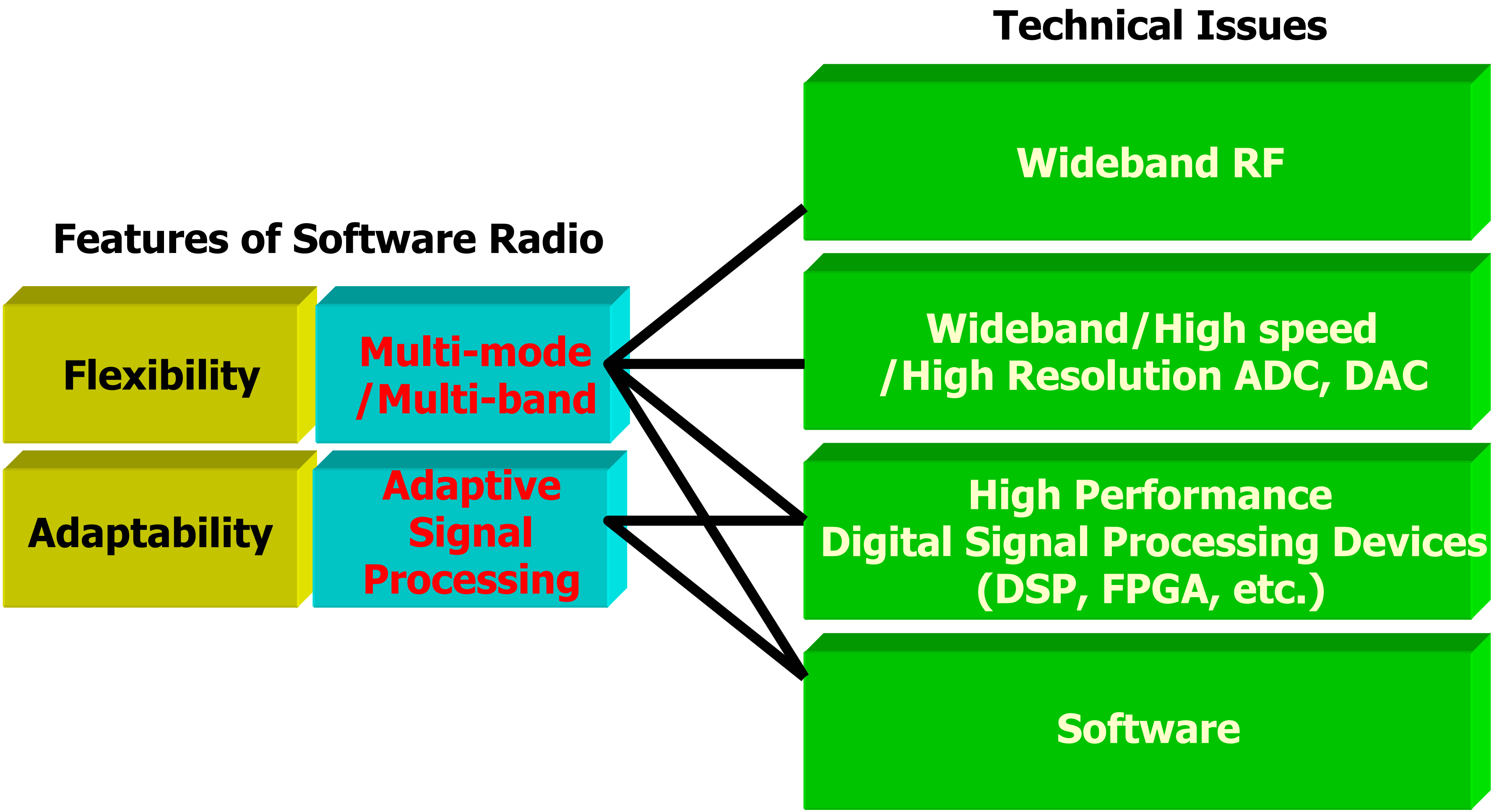


Definition of SDR Technology

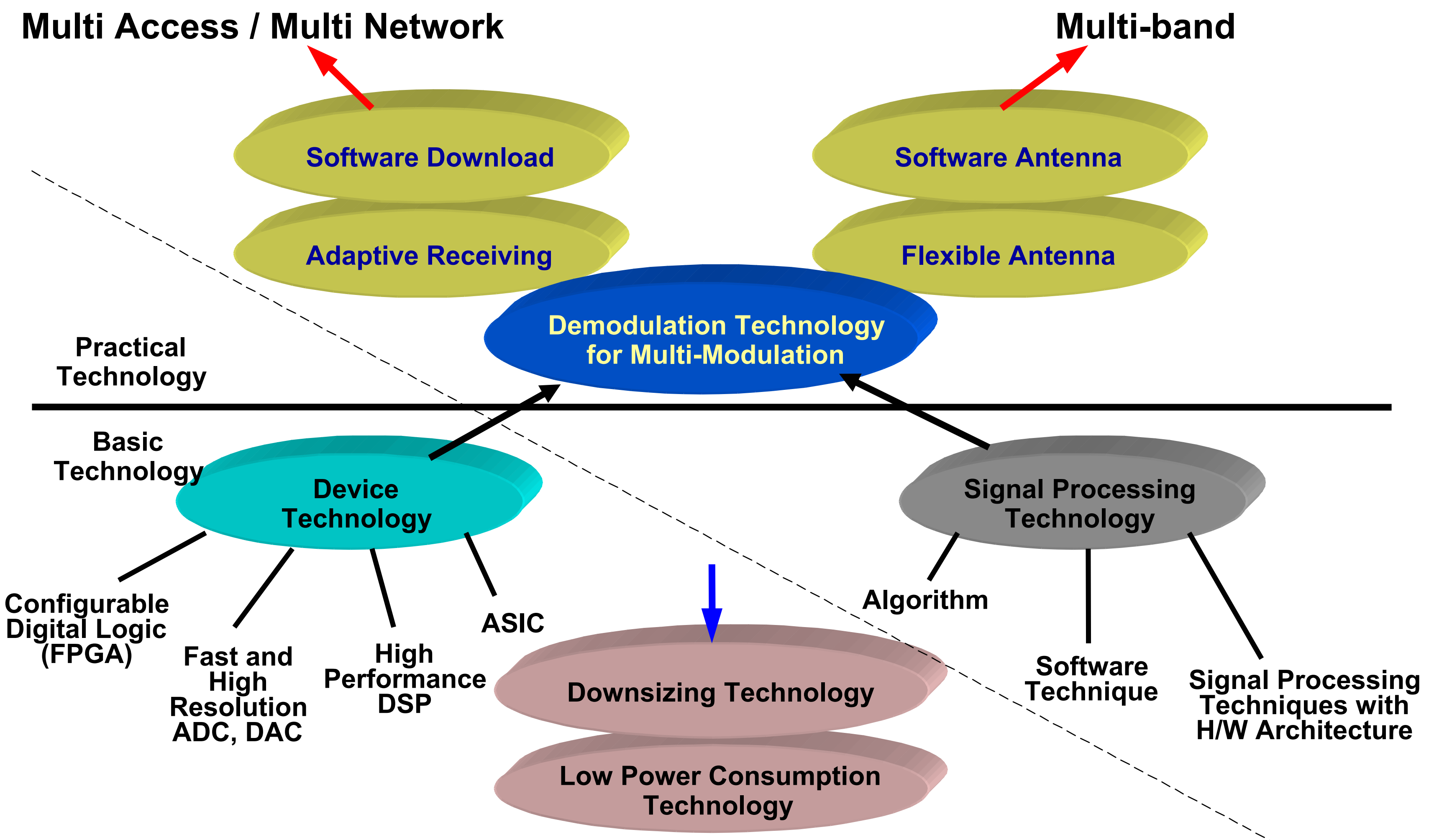
"The process of managing complexity whilst maximizing flexibility by using the techniques of non real time software engineering in hard real time domain."



Core Technologies for SDR (cont.)



Core Technologies for SDR



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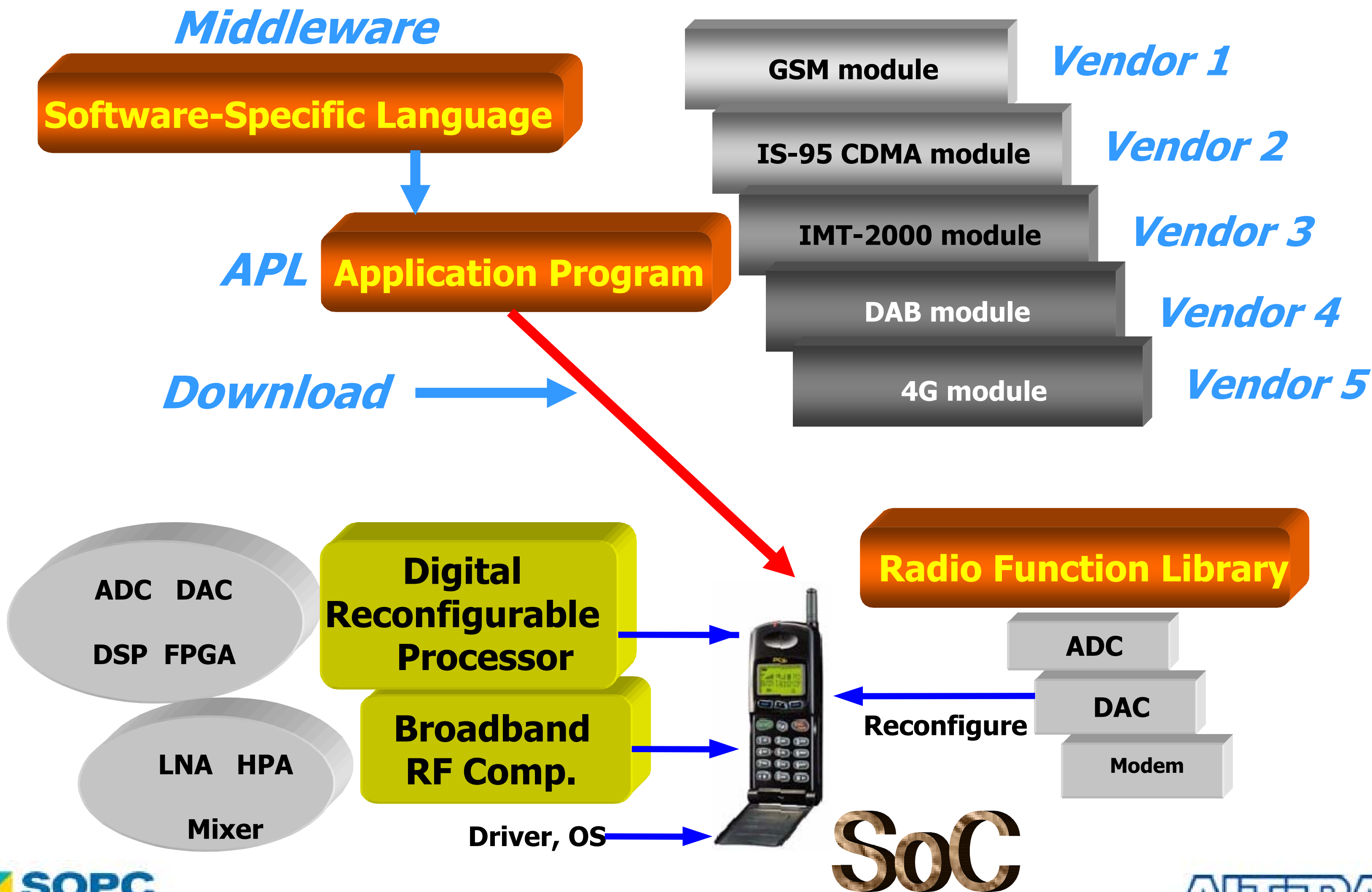
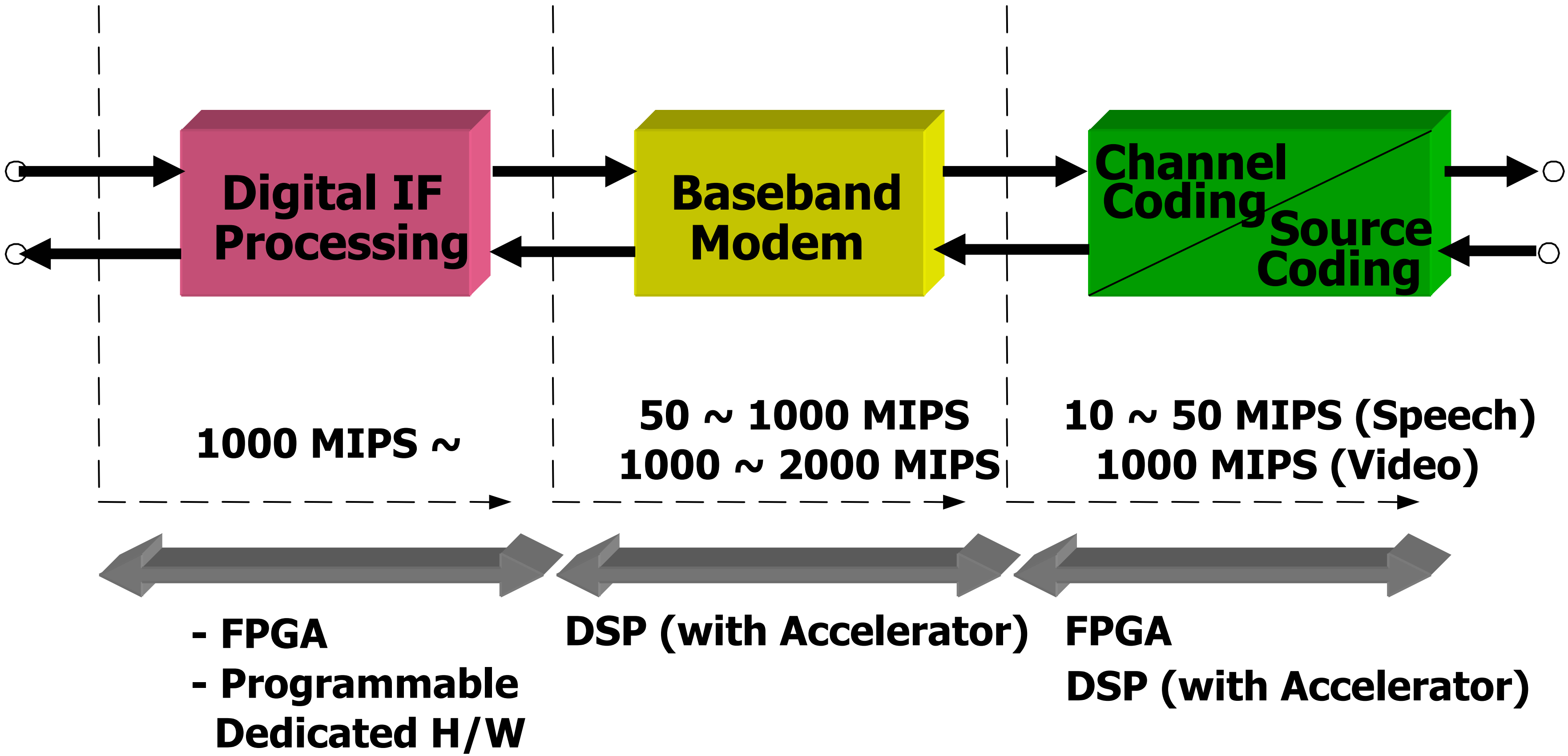
Functionalities for SDR-based Handset



Digital Hardware Resources for SDR



"More sophisticated signal processing algorithms must be employed to increase throughput over limited frequency resource"

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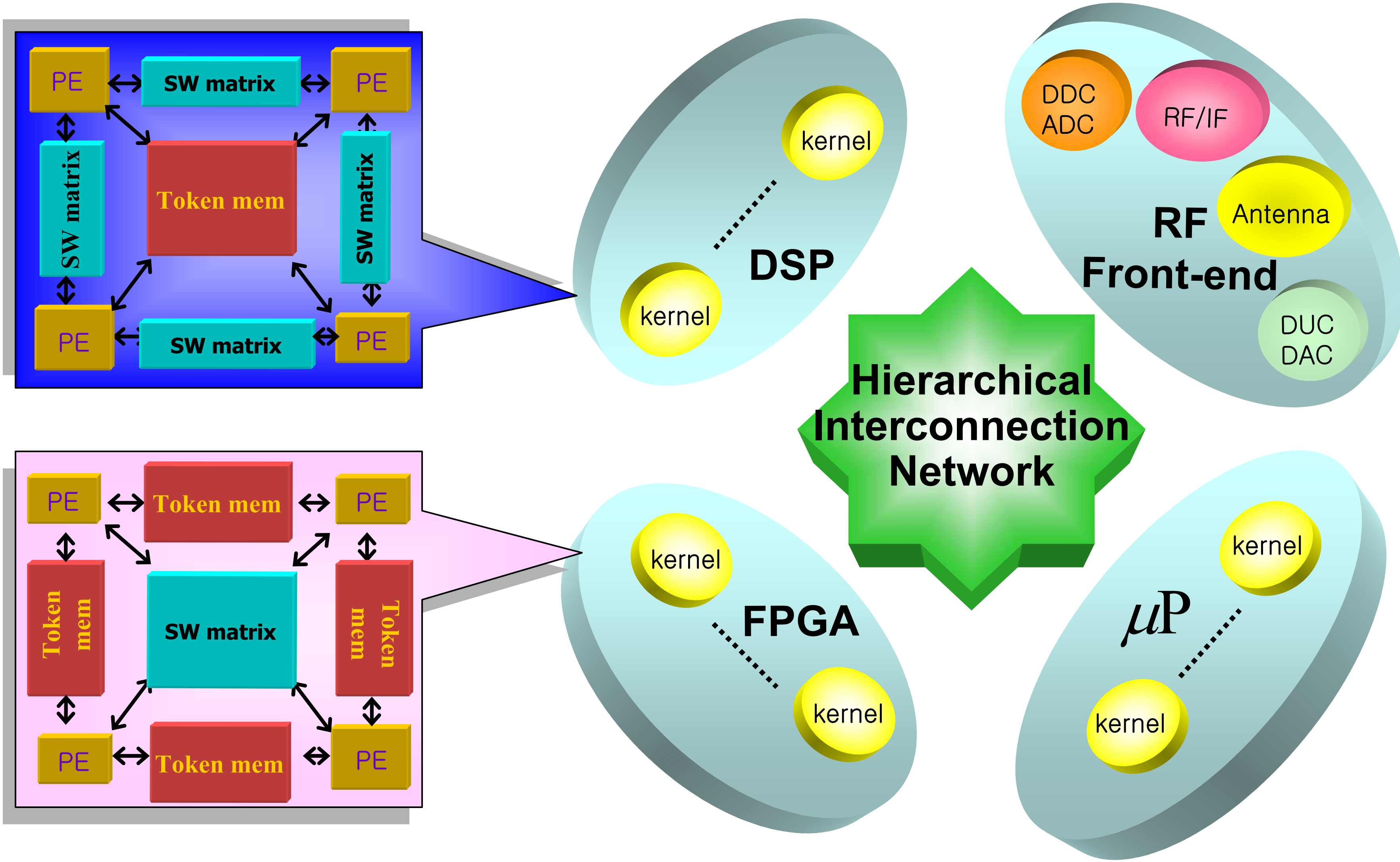
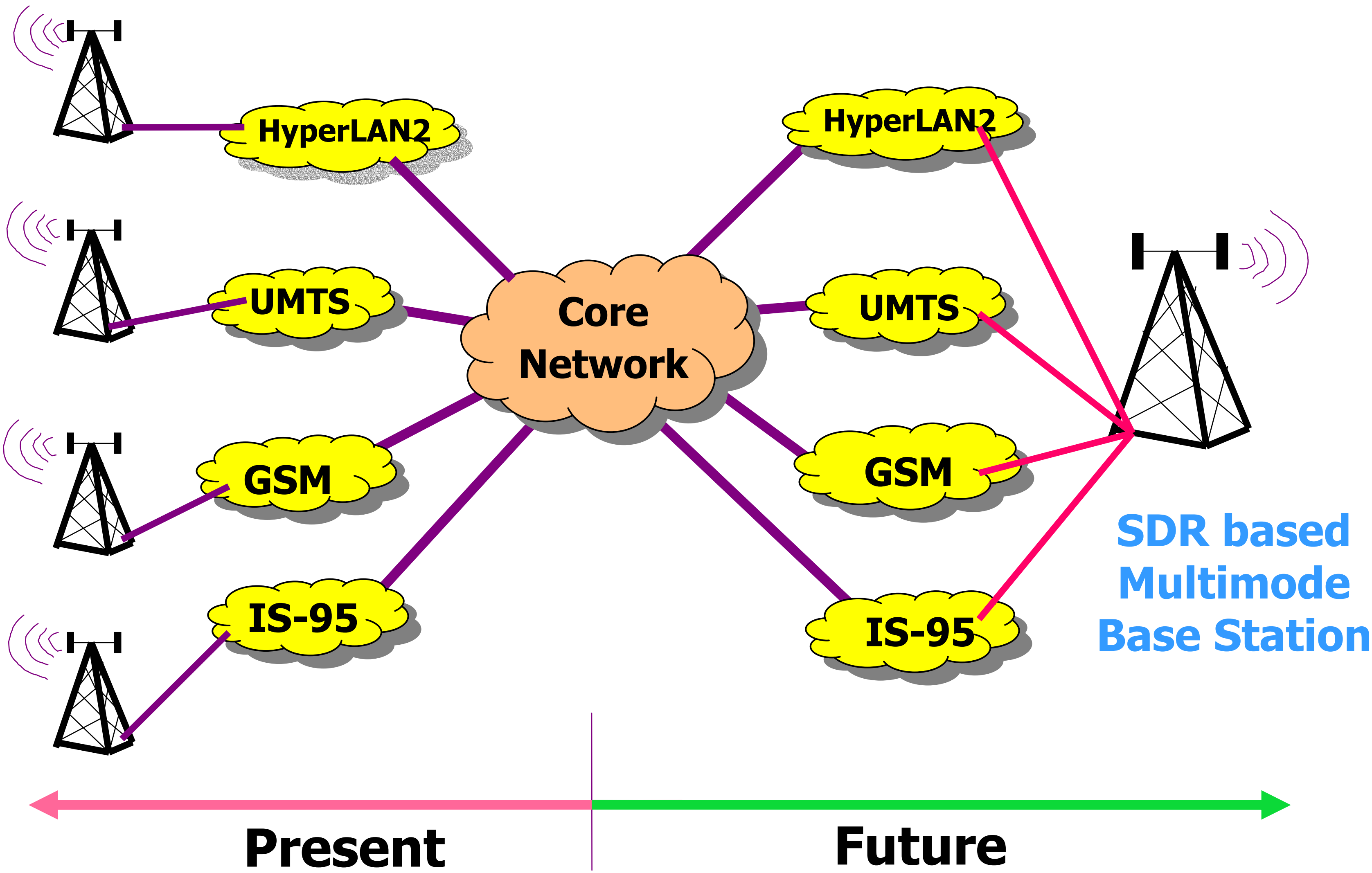
Generic Structure of SDR Platform



Enhancement of Radio Access by SDR



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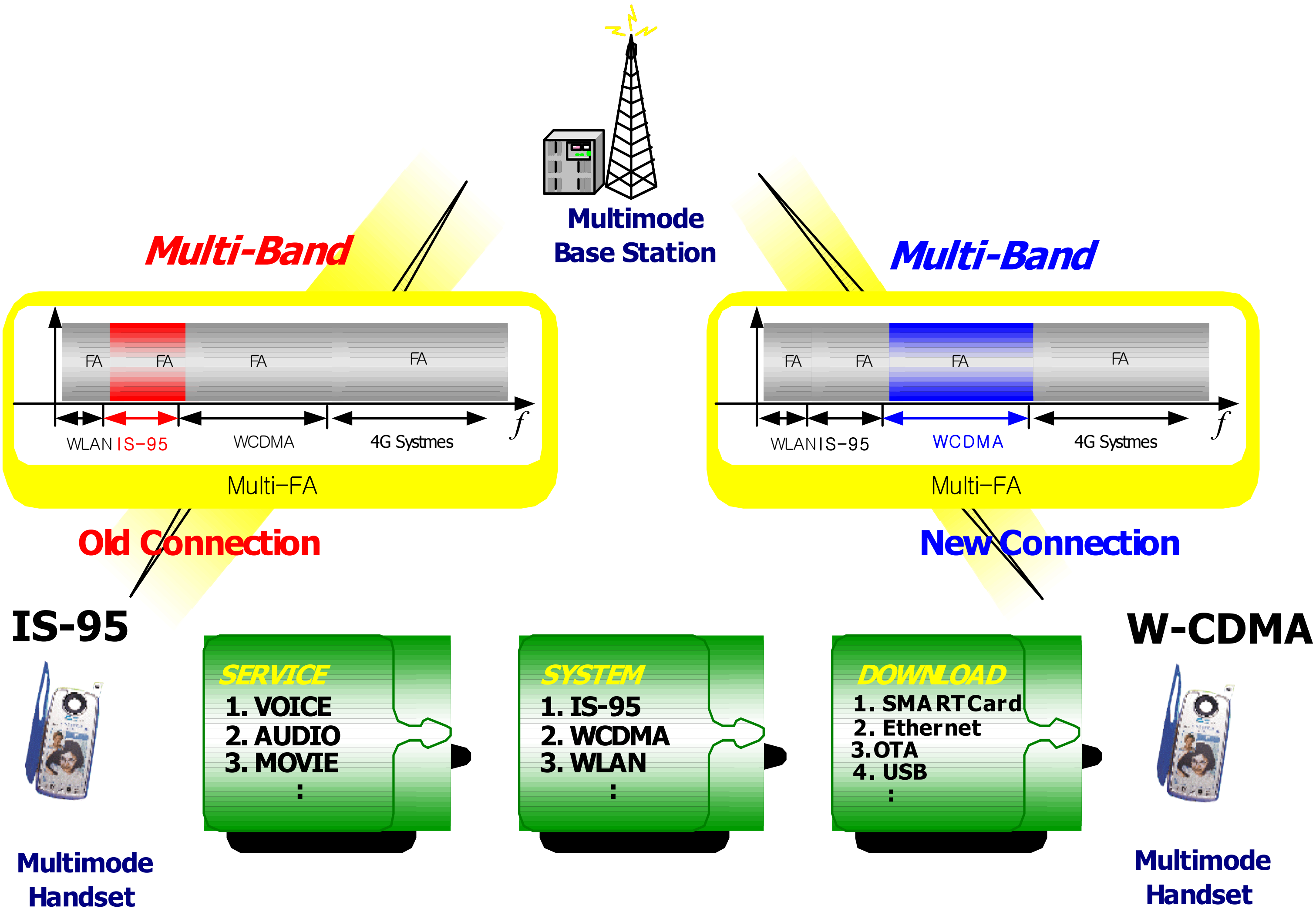
SDR-based Multimode BS and Handset



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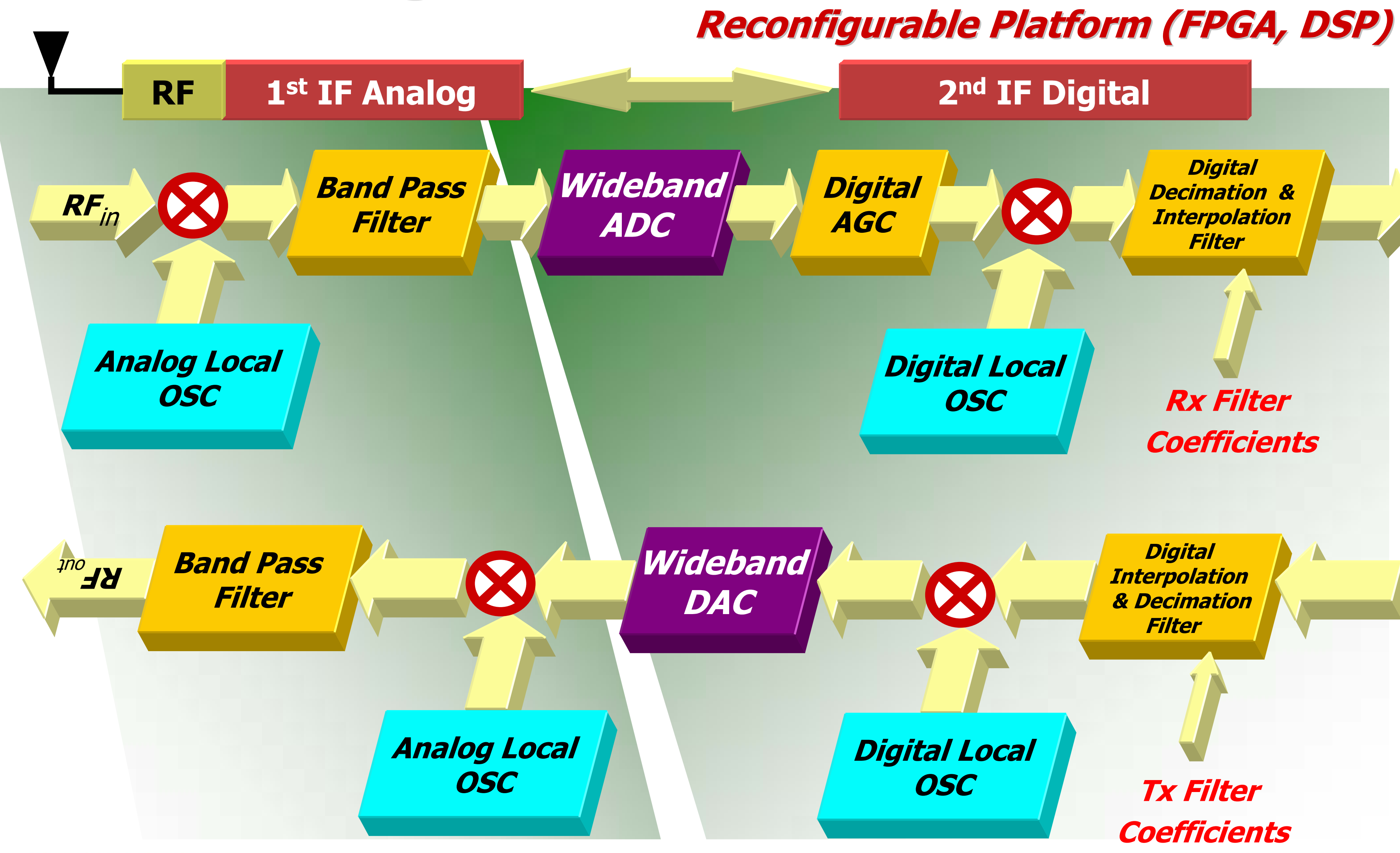
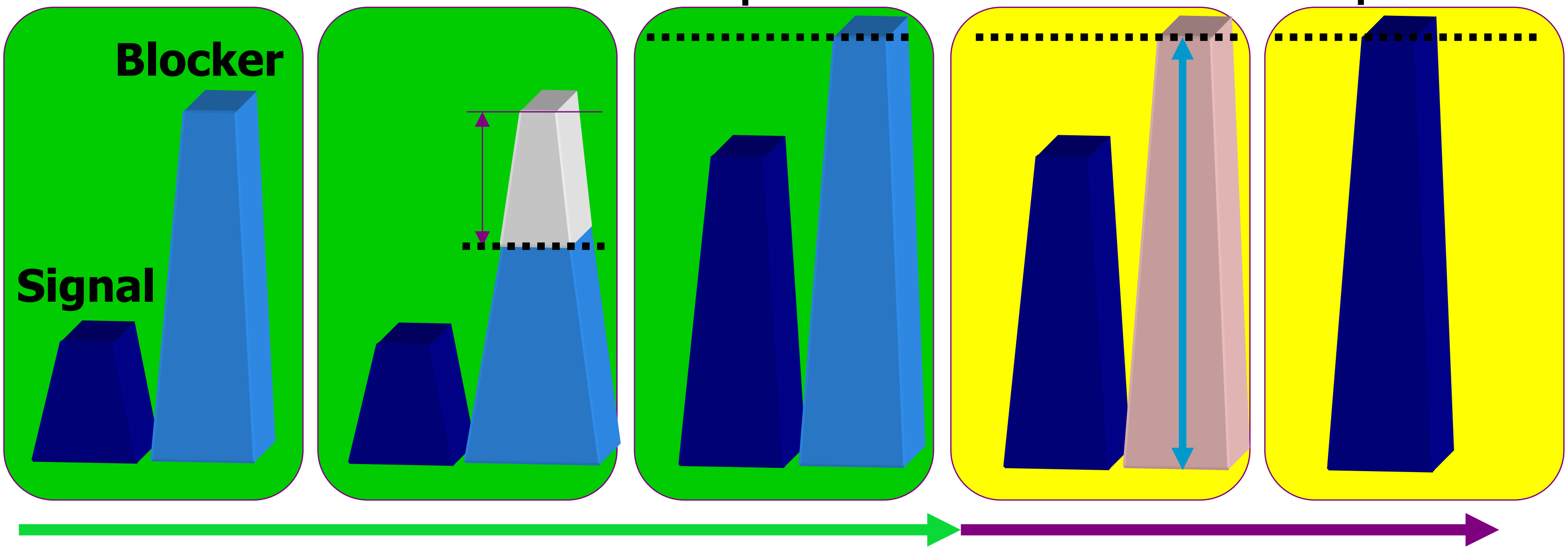
What is Digital IF?



Blocker Rejection and Digital AGC

	Analog Attenuation	Analog AGC Output Level	Digital Attenuation	Digital AGC Output Level



Analog Processing **Digital Processing**

RF Input	Analog SAW filter output	Analog AGC output	Digital filter output	Digital AGC output

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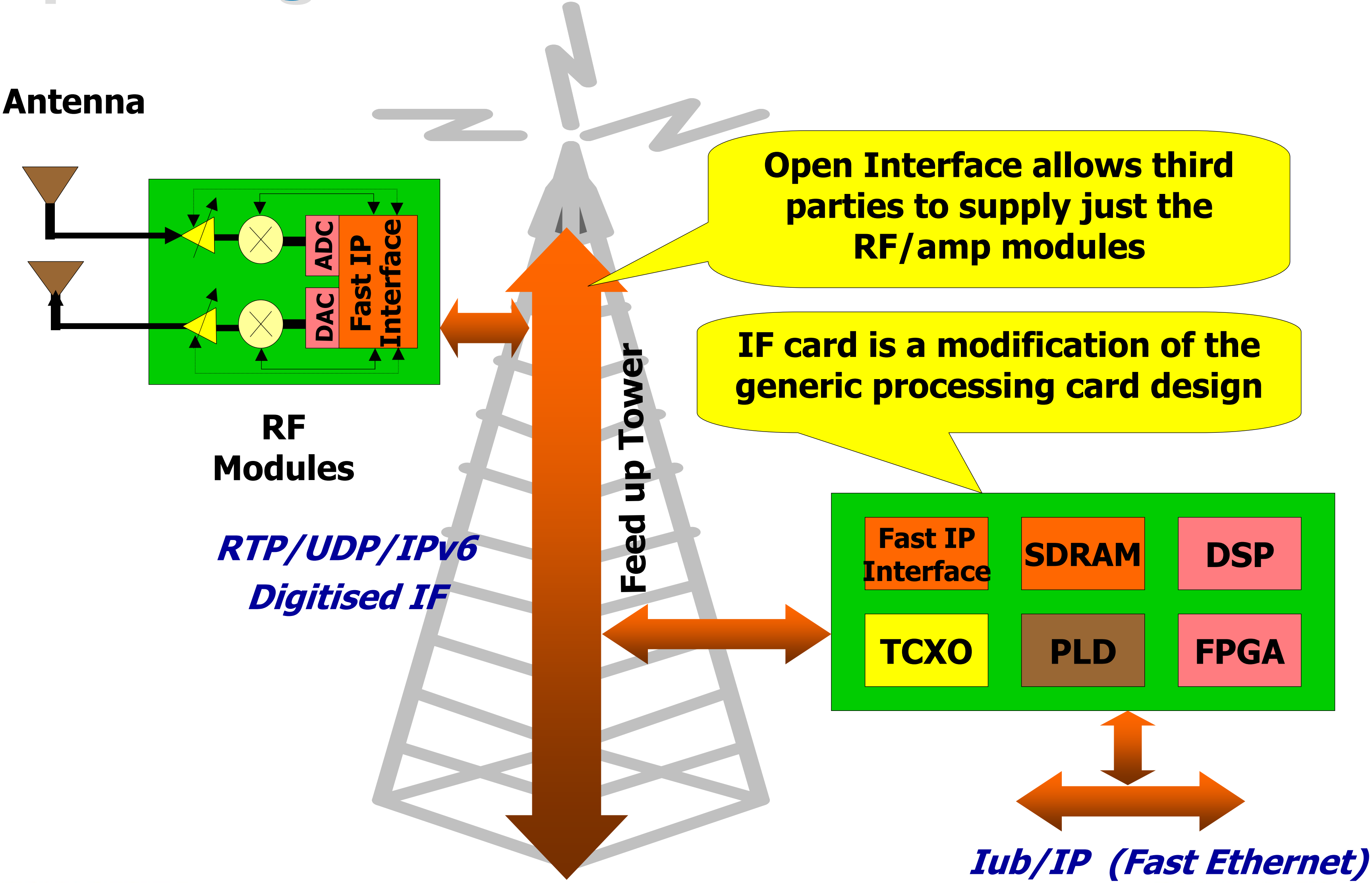
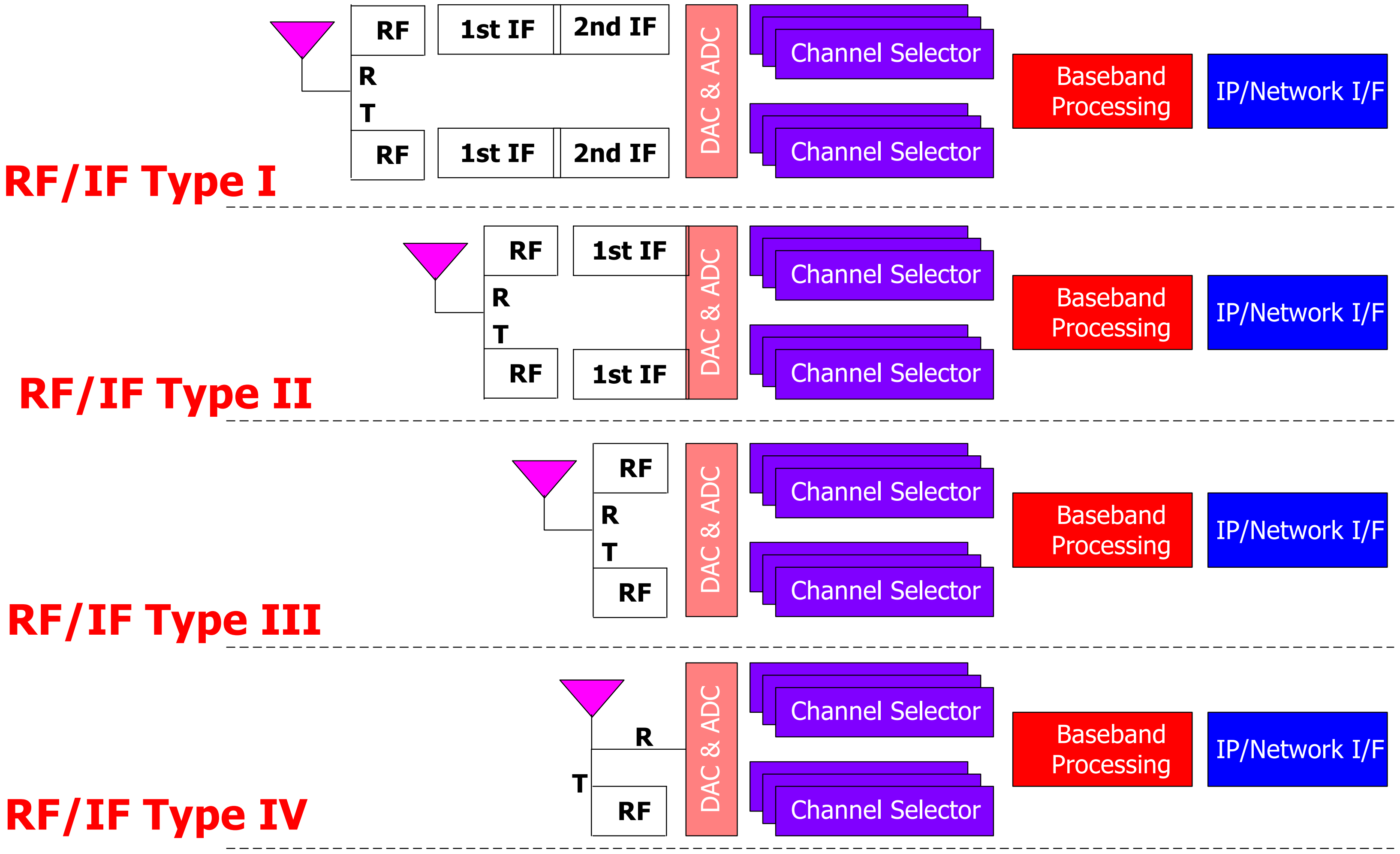
Open Digital IF Architecture for BS



Evolution of Digital RF/IF Technique



Advantages of Digital IF

- More digital components in Analog Front End
- More digitally tunable components
- More strong to adjacent co-channel interference
- Easy to adapt sophisticated digital signal processing in IF

  (eg., Adaptive pre-distorter, IF bandpass filtering, etc)
- Easy to upgrade by software to fit released spec.
- More robust to aging problem
- Cost effective by reducing analog components

Components for implementing Digital IF

Analog IF	*Digital IF*
Amplifier	Digital Multiplier
Mixer	Digital Multiplier & LUT
Local Oscillator	Numerical Oscillator
Filter	Digital Filter & RAM
	ADC,DAC

Characterisitics of Analog-to-Digital Converte

- Sampling Speed
  - As increasing
    - **Processing bandwidth is widened**
    - **Processing gain for baseband is increased**
    - **Power consumption is increased**
  - As decreasing
    - **Power consumption is decreased**
    - **Suitable for handset with using Zero IF technique**
- Bit Resolution
  - **It determines dynamic range of ADC (N bit ADC ~ 6*N [dB])**
  - **ENOB(Effective Number of Bits)**
    - **It is less than 6*N [dB] Dynamic Range due to harmonic noise**
- Analog Input Bandwidth
  - **It should be greater than Nyquist Freq. for bandpass sampling**

Considerations for ADC Circuit Design

- Input center frequency is set to $f_{Nyquist}$ /2 due to mitigate
  - **1/f Noise around DC**
  - **Image around $f_{Nyquist}$**
- Isolation between analog input and digital circuit
  - **Isolation between analog components and digital components**
  - **Isolation between analog ground and digital ground**
- Input Clock for ADC should have
  - **Very low noise**
  - **Be isolated with the clock for digital circuit**
  - **Be differential clock to alleviate noise**

Performance of current and future ADCs

Feature	Performance Range	
	Semiconductor-Based	Superconductor-Based
Frequency	Up to 200 MHz	Up to > 2 GHz
Resolution	10 to 14 bits quoted (ENOB typically 2 to 4 less)	14 to 24 bits ENOB
Spur Free Dynamic Range	60 to 90 dB	100 to 150 dB
Sensitivity	N/A (normally post LNA)	-120 to -180 dBm

Characterisitics of Digital-to-Analog Converter

- Sampling Speed
  - **determines available output frequency**
- SFDR(Spur Free Dynamic Range)
  - **determines output dynamic range with considering Harmonic Distortion**
- Inverse Sinc Filter
  - **is required for the flatness of inband frequency characteristic**
- Image Rejection Filter
  - **Is required for unintentional harmonic image**

Bandpass Sampling Technique (cont.)

Bandpass Sampling

The technique of under-sampling a modulated signal to achieve frequency translation via intentional aliasing.

Sampling Conditions

$$0 < F_{IF} - \frac{BW_I}{2} \qquad\qquad F_{IF} + \frac{BW_I}{2} < \frac{F_S}{2}$$

Bandpass Sampling Technique (cont.)

Frequency Selection Rule

IF frequency in information bandwidth which is occurred from folding can be determined from sampling frequency Fs and center frequency Fa.

$$\text{If } fix\left(\frac{F_a}{F_s/2}\right) \text{is} \begin{cases} \text{even}, & F_{IF} = rem(F_a, F_S) \\ \text{odd}, & F_{IF} = F_S - rem(F_a, F_S) \end{cases}$$

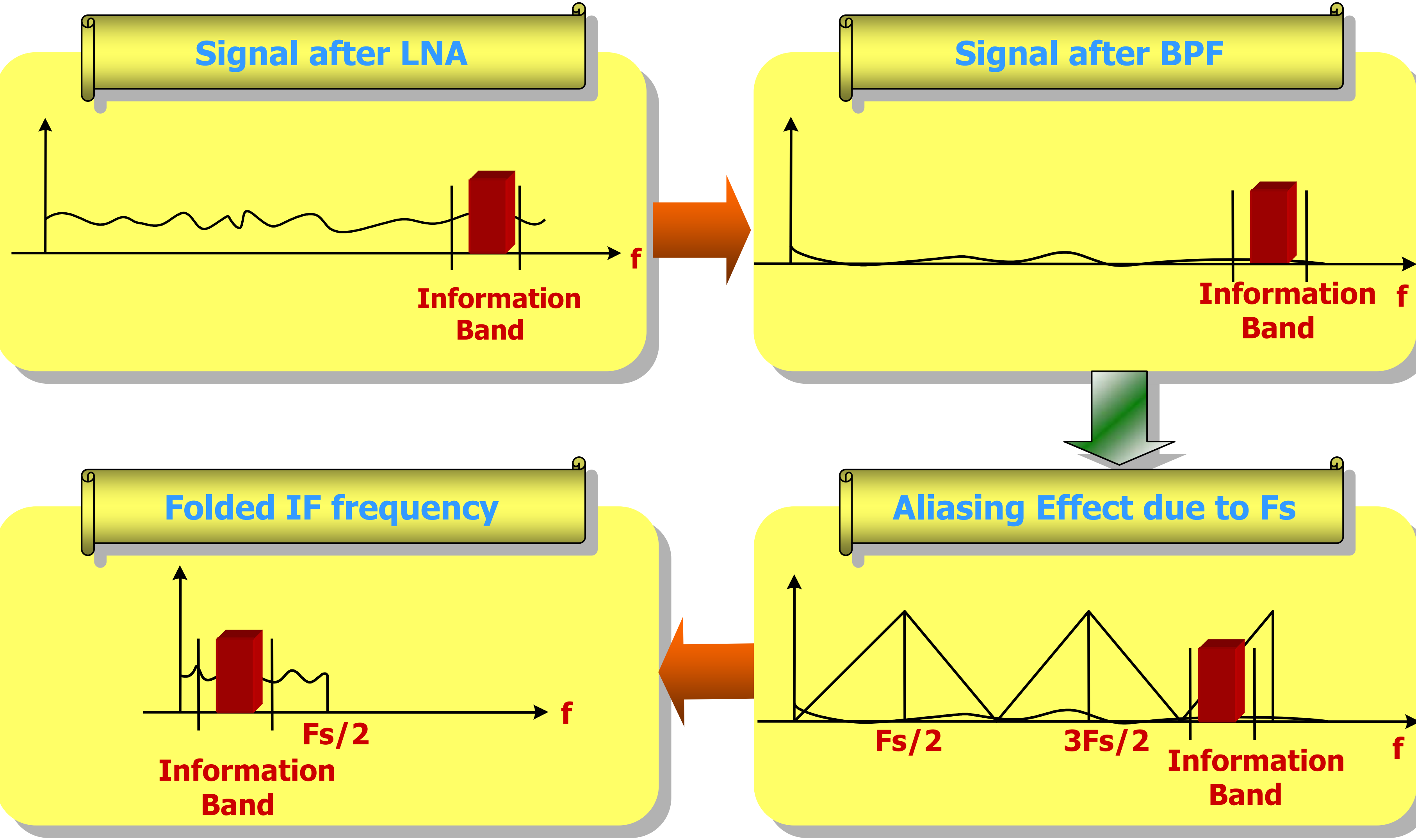
where F_a = input frequency to ADC

F_{IF} = intermediate frequency

$fix(\text{a})$: truncated portion of argument a

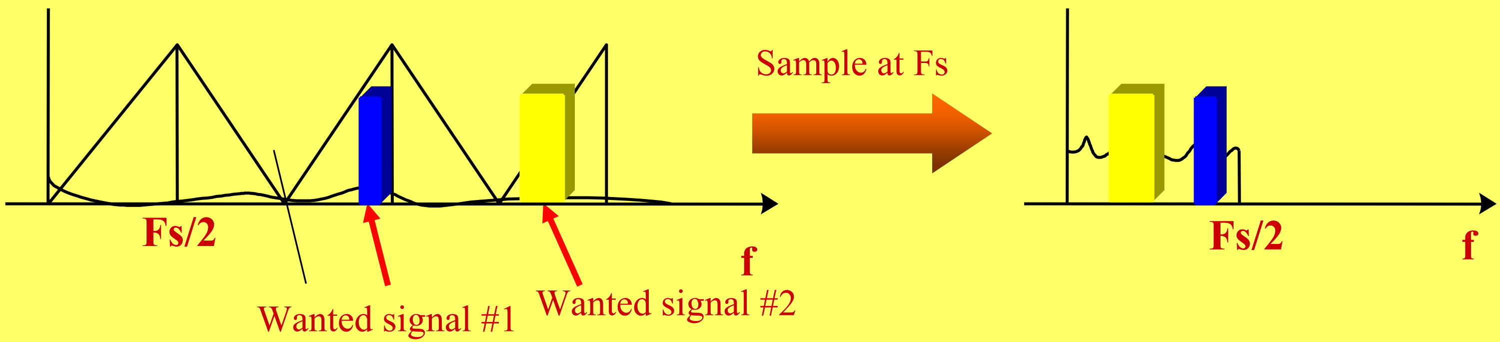
$rem(\text{a}, \text{b})$: remainder after division of a by b

Bandpass Sampling Technique



Bandpass Sampling for Multiband Signa

Bandpass Sampling for Multiband Signal

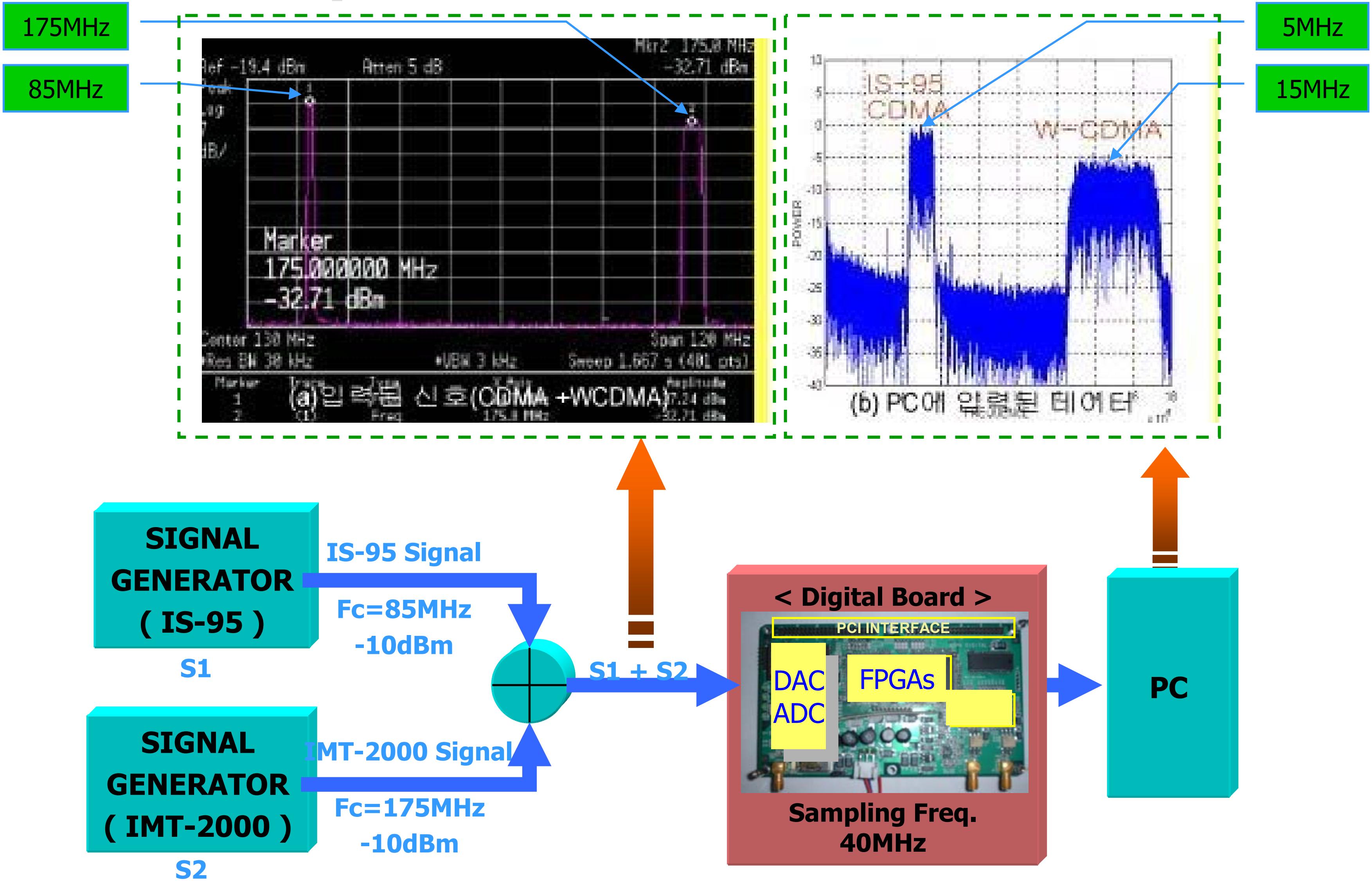


Sampling Condition

Multiband signals resulted from folding effect should not be overlapped each other in information band.

$$|F_{IF_1} - F_{IF_2}| \geq \frac{BW_{I_1} + BW_{I_2}}{2}$$

An Example : IS-95 and W-CDMA



Multimode Input (IS-95, W-CDMA, W-LAN)

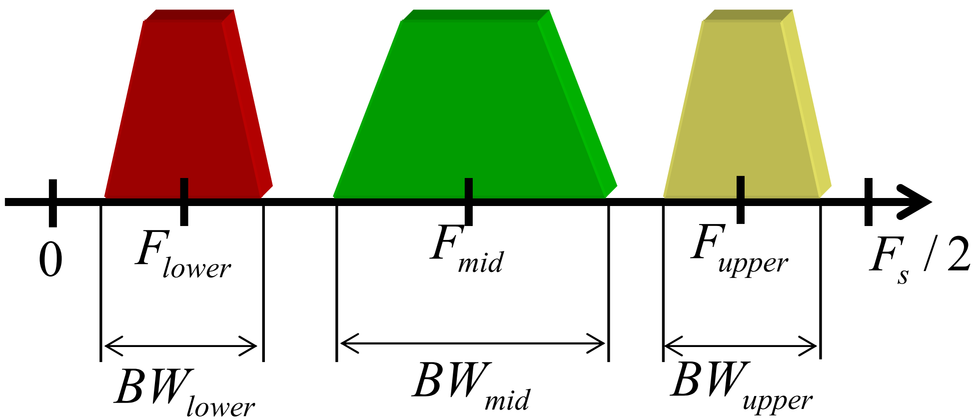
- Signals considered here
  - **IS-95**
    - **Bandwidth : 1.25 MHz/1FA**
    - **Chip rate : 1.2288 Mcps**
  - **W-CDMA**
    - **Bandwidth : 5 MHz/1FA**
    - **Chip rate : 3.84 Mcps**
  - **IEEE 802.11a W-LAN**
    - **Effective Bandwidth : 16.6MHz**
    - **Transmission Bandwidth : 20 MHz**
- Total information bandwidth : 26.25 MHz

IF Freq. Plan for IS-95, W-CDMA, W-LAN

- Conditions

$$0 < F_{lower} - \frac{BW_{lower}}{2} \qquad F_{upper} + \frac{BW_{upper}}{2} < \frac{F_S}{2}$$

$$|F_{mid} - F_{lower}| \geq \frac{BW_{mid} + BW_{lower}}{2} \qquad |F_{mid} - F_{upper}| \geq \frac{BW_{mid} + BW_{upper}}{2}$$

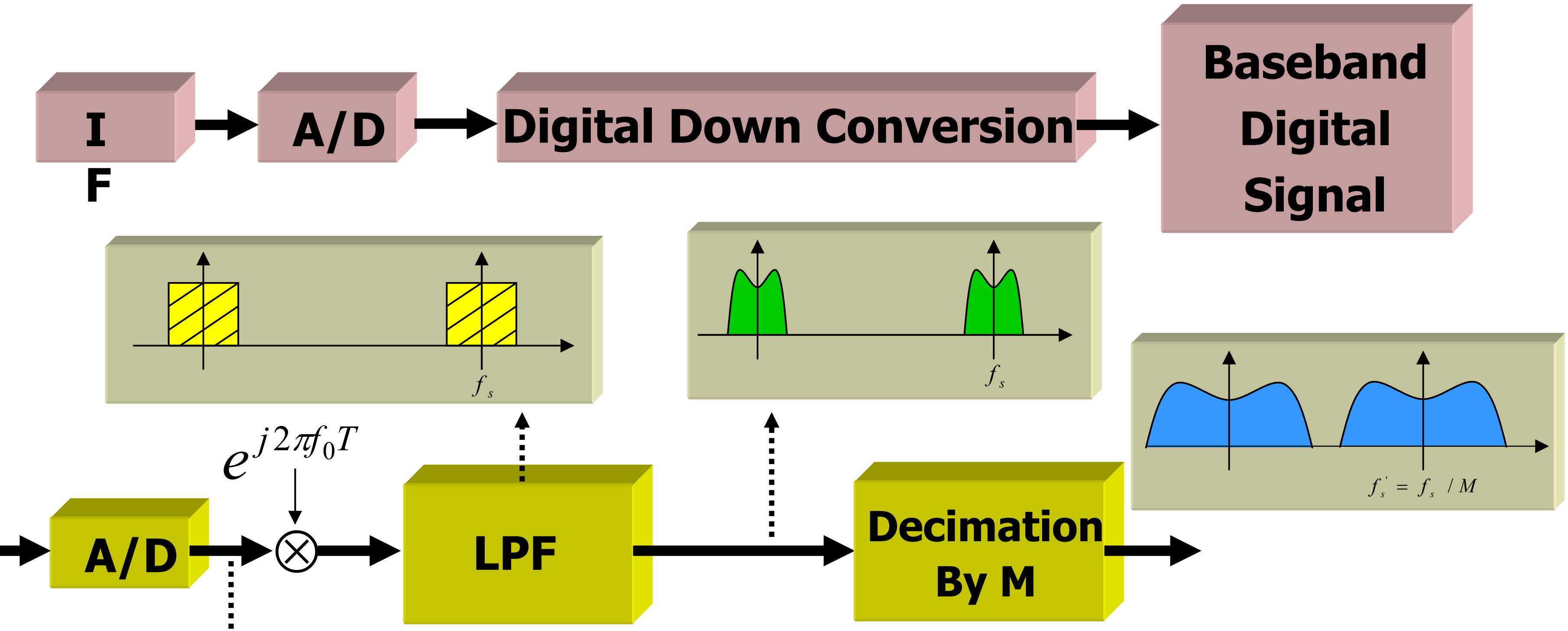


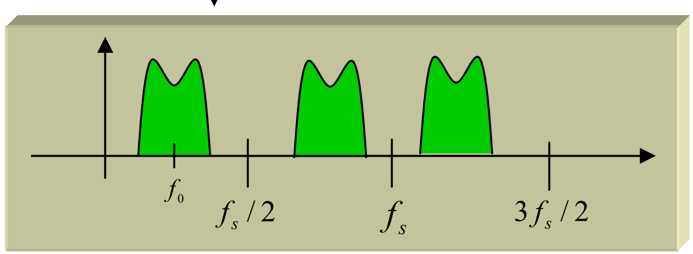
Selected IF Frequency Plans

- IF frequency band : 70~130 MHz
- Sampling Frequency : 65 MHz

IF Frequency (MHz)			Digital Frequency (MHz)		
IS-95	W-CDMA	W-LAN	IS-95	W-CDMA	W-LAN
128	123	109	2	7	21
127	122	88	3	8	23
119	125	107	11	5	23
98	104	118	32	26	12
96	126	84	31	4	19
74	126	109	9	4	21

Digital IF Down Conversion



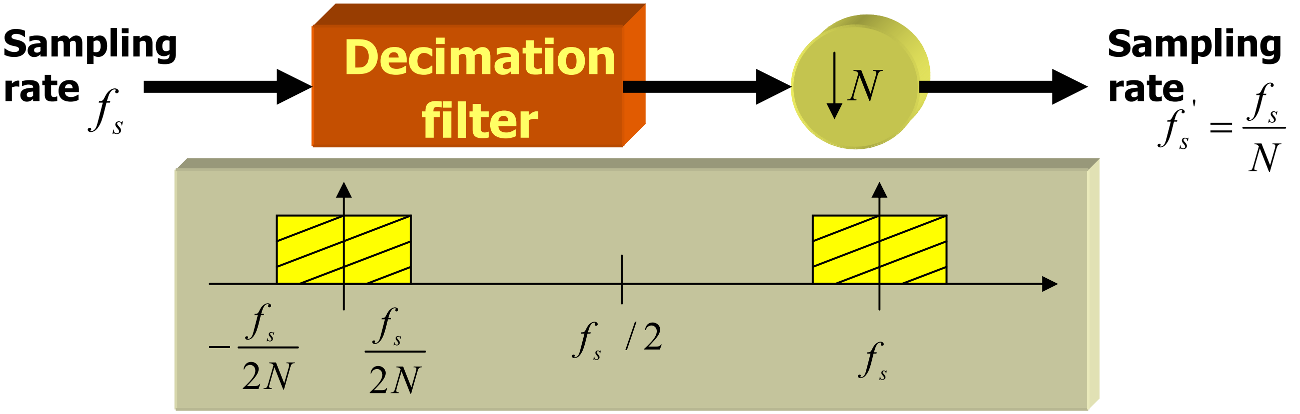


- **Low Pass Filter Design (Decimation Filter);**

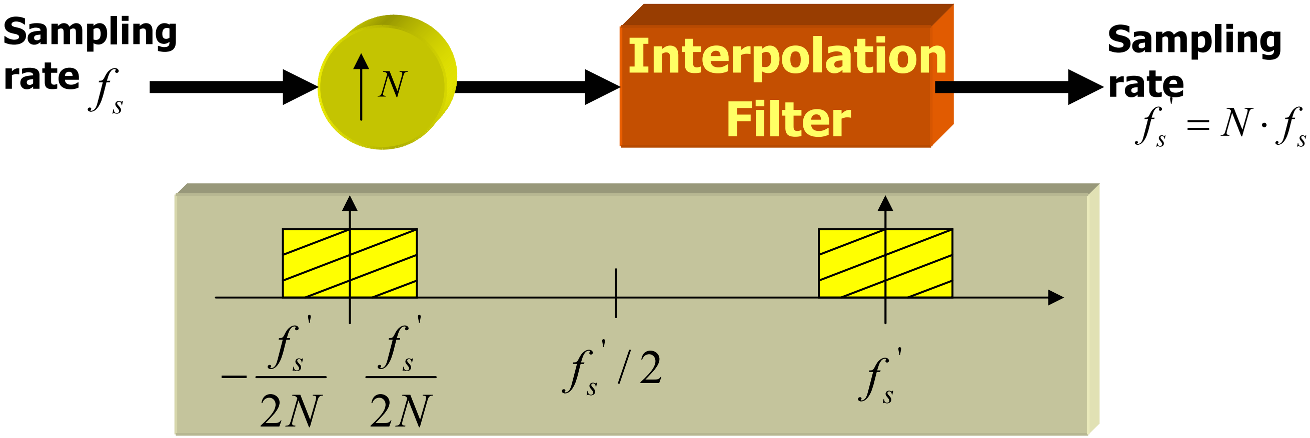
CIC Filter + Half-Band Filter

Decimation and Interpolation process

- **Decimation Process** N : Decimation ratio



- **Interpolation Process** p : Interpolation ratio



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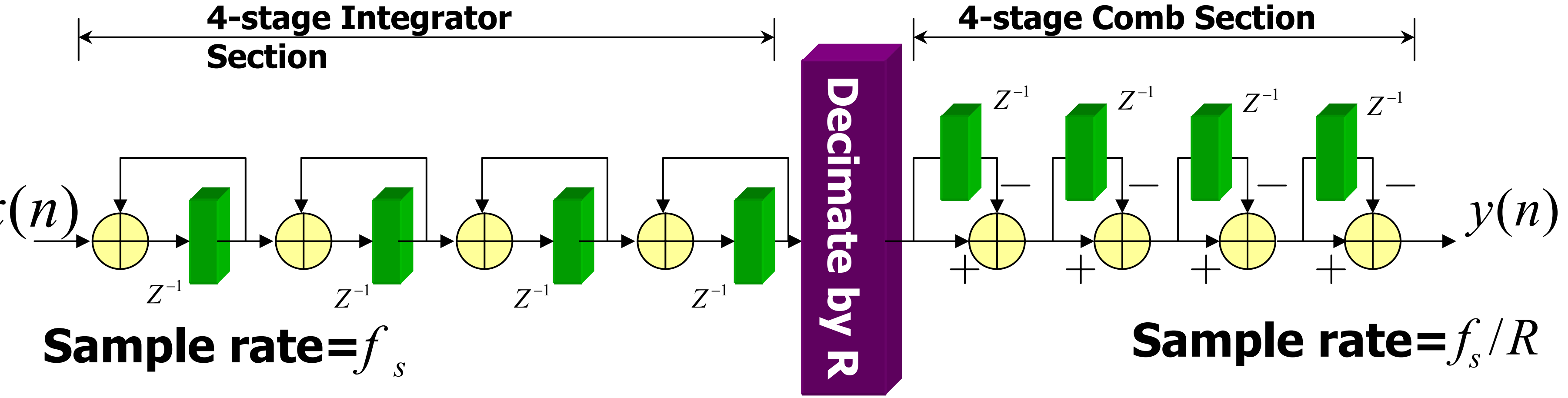
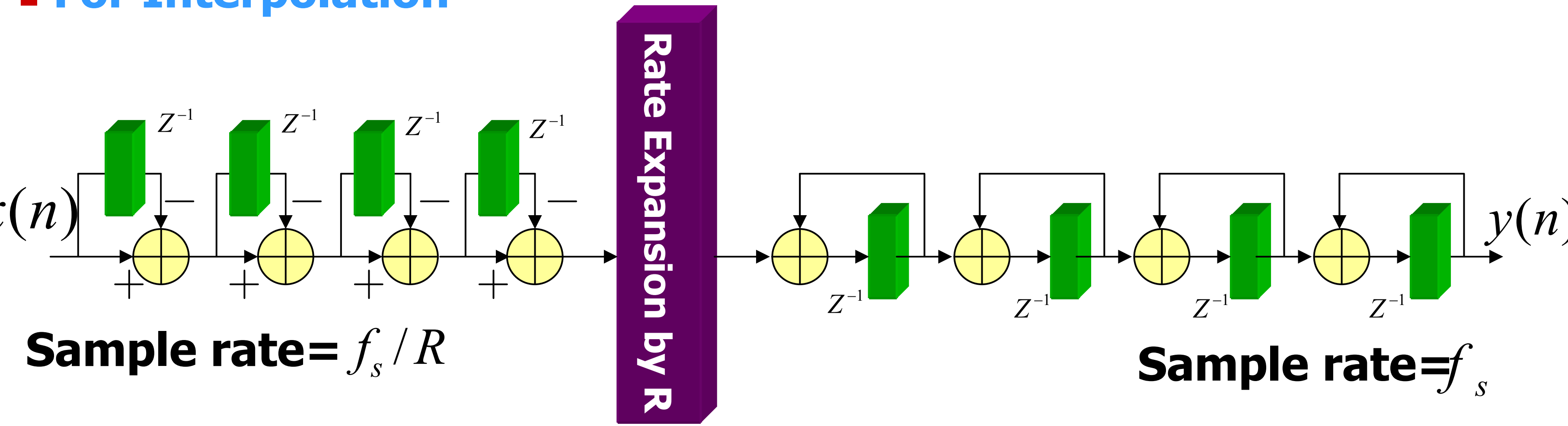
Structure of CIC Filter

- **For Decimation**



- **For Interpolation**



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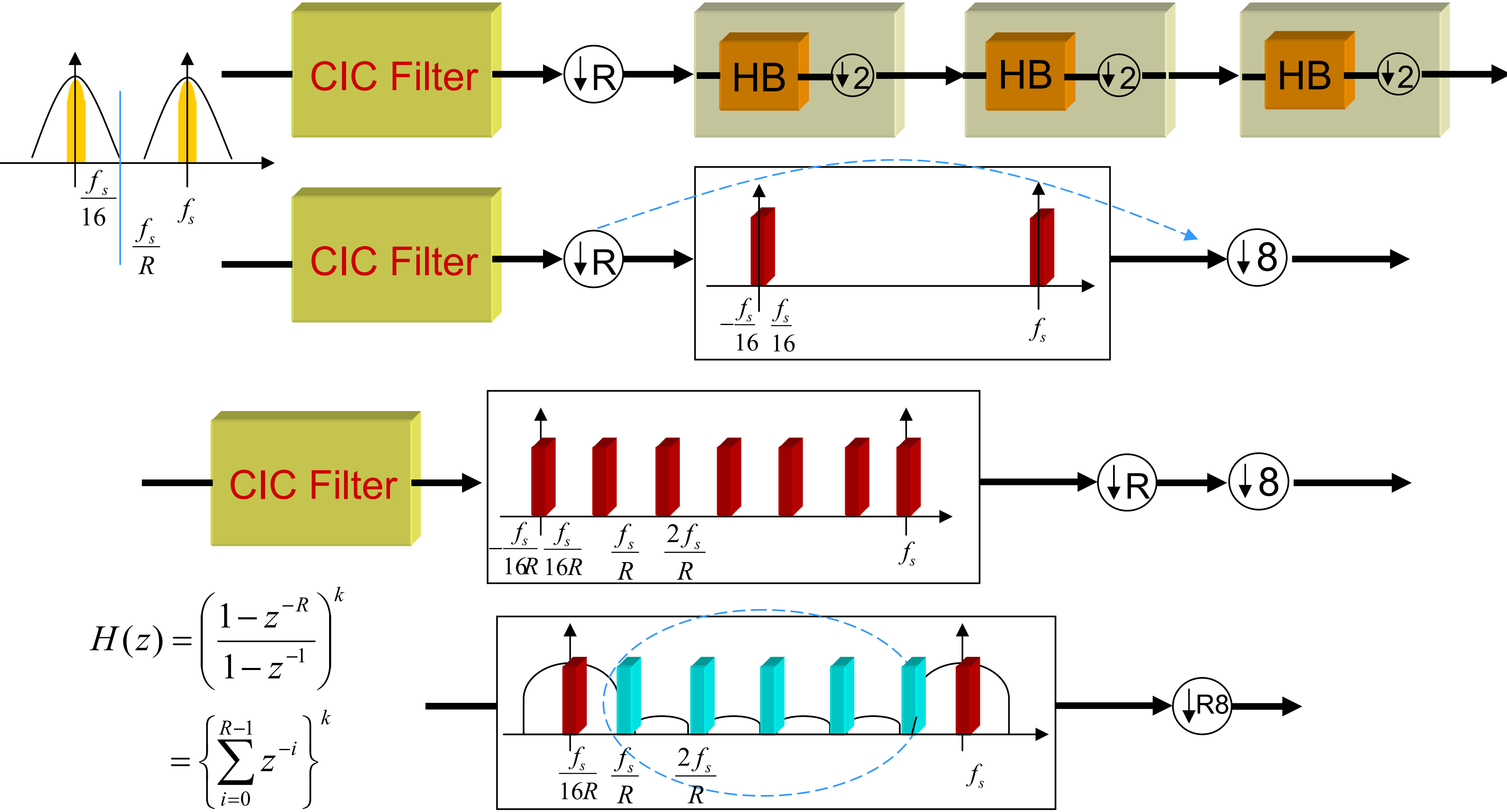
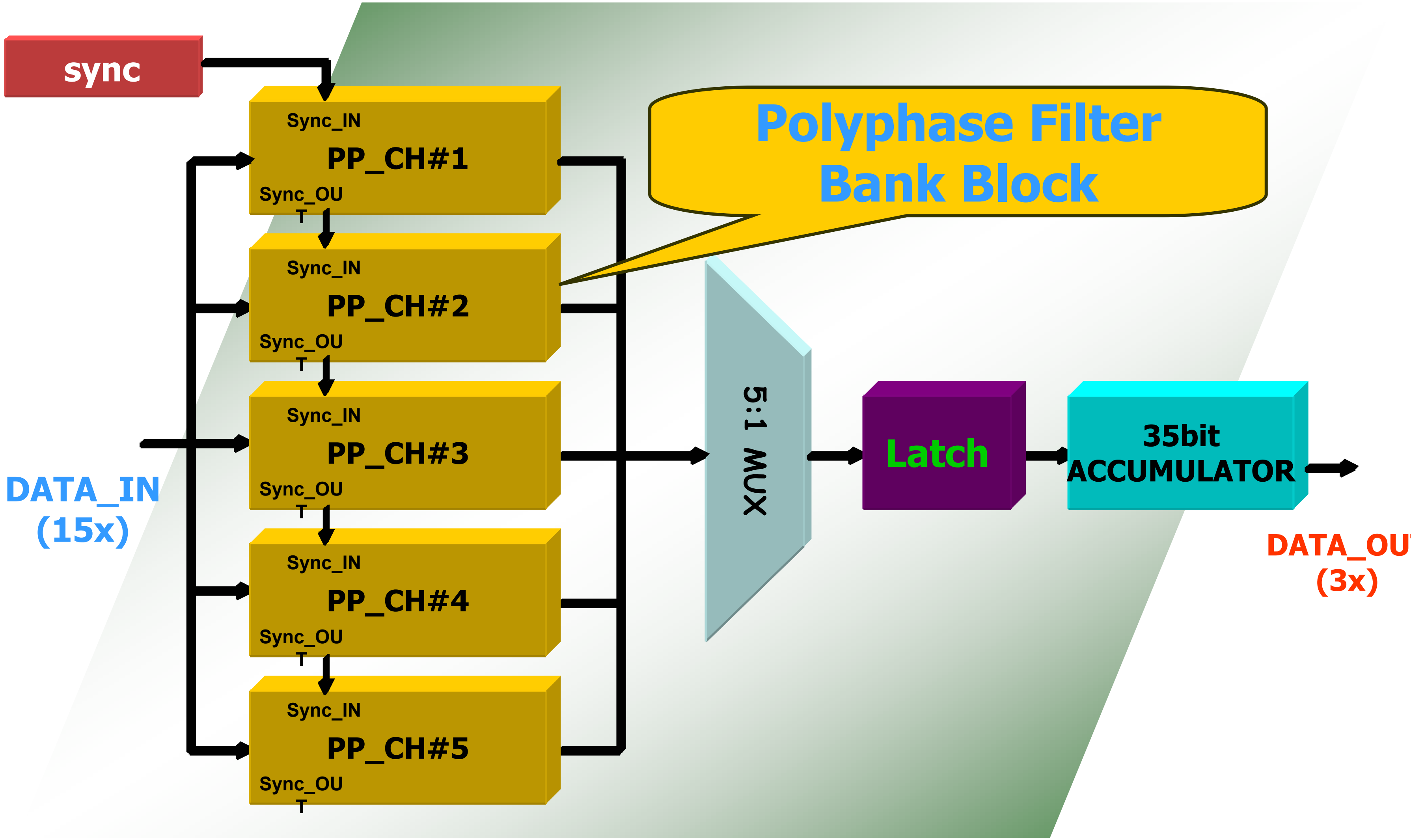
Decimation Filter using CIC & HB Filter



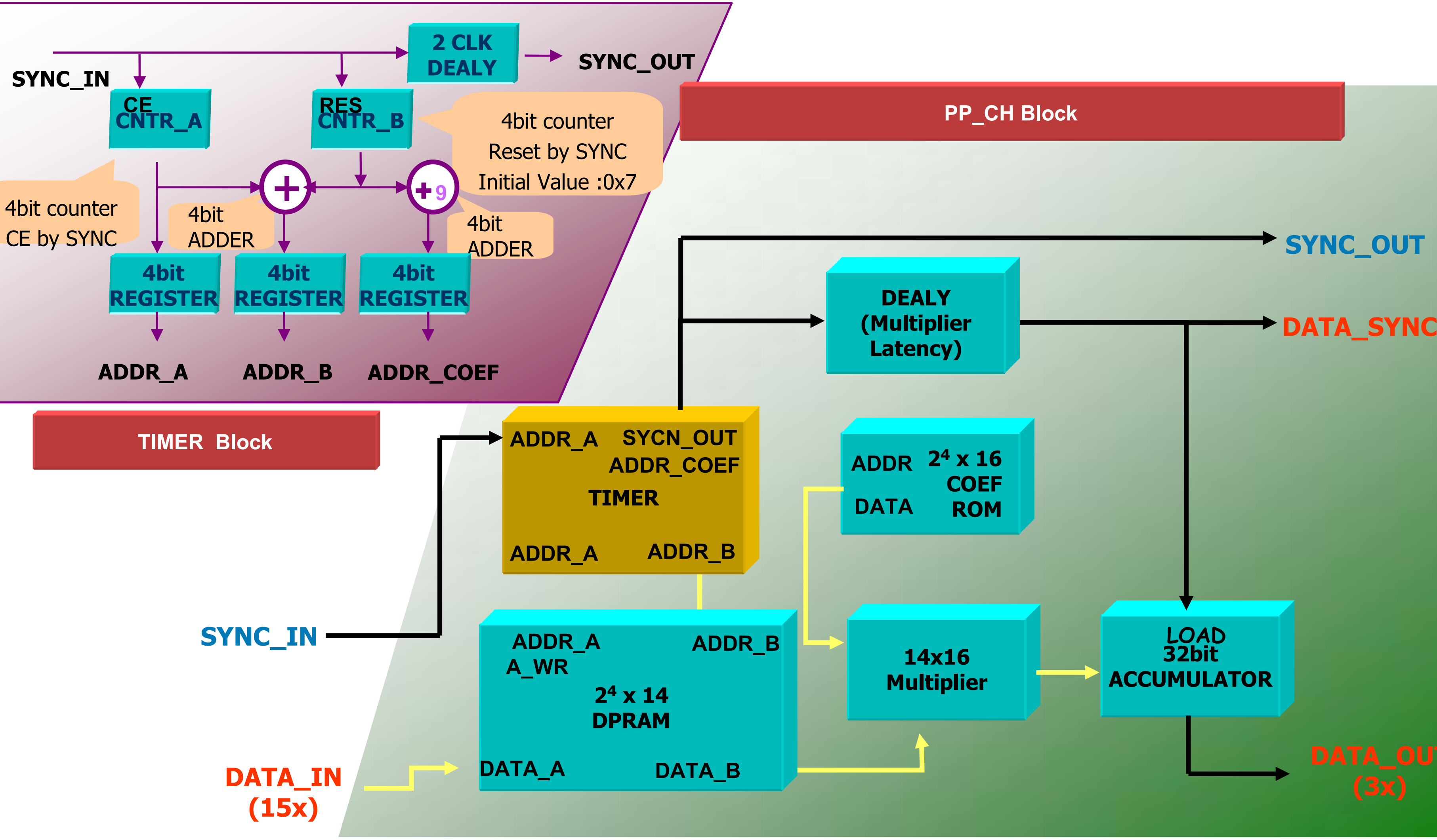
$$H(z) = \left(\frac{1 - z^{-R}}{1 - z^{-1}} \right)^k$$

$$= \left\{ \sum_{i=0}^{R-1} z^{-i} \right\}^k$$

Efficient FIR Filter Processing (cont.)



Efficient FIR Filter Processing



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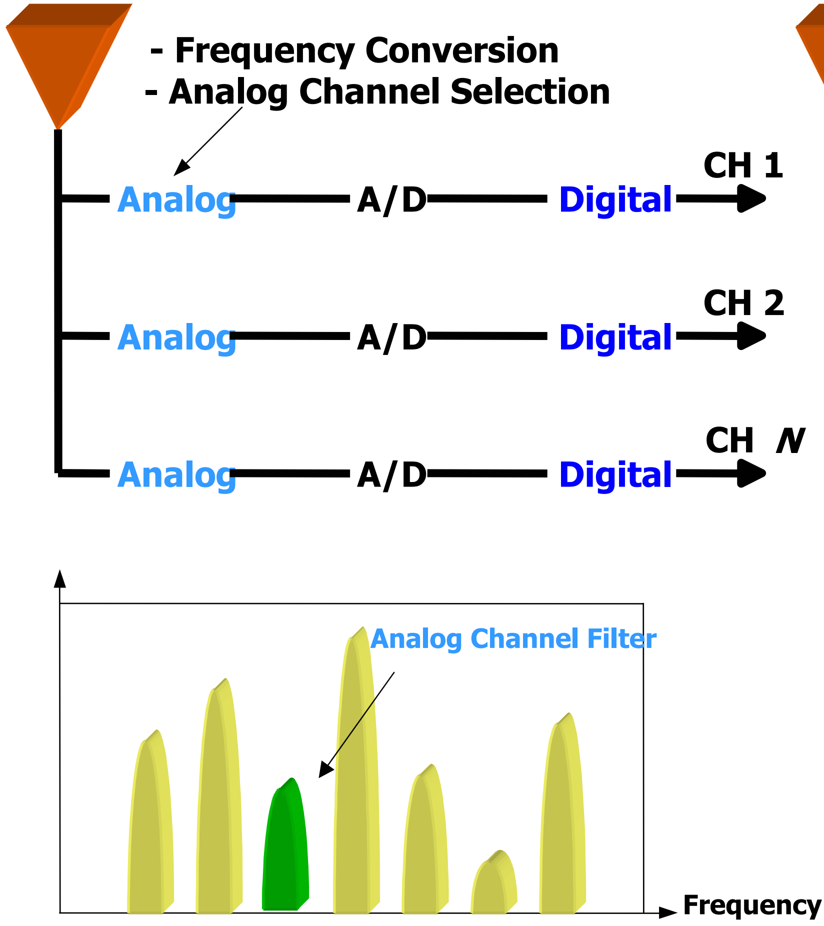
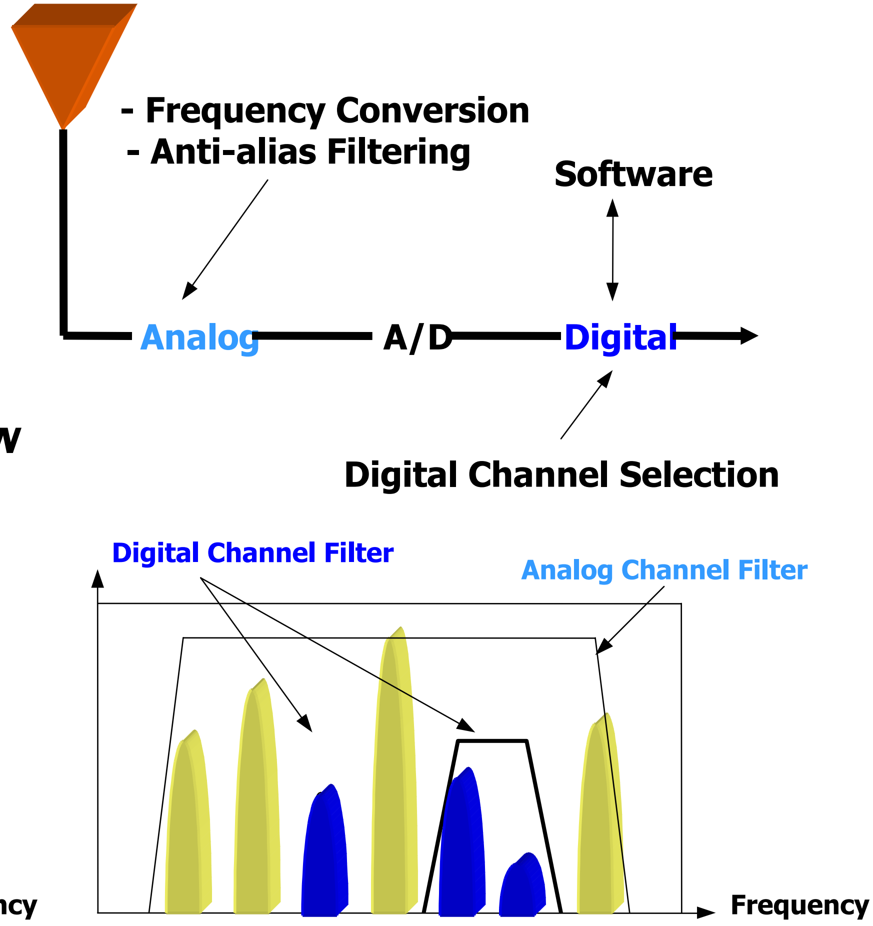
Digital IF Channelizer

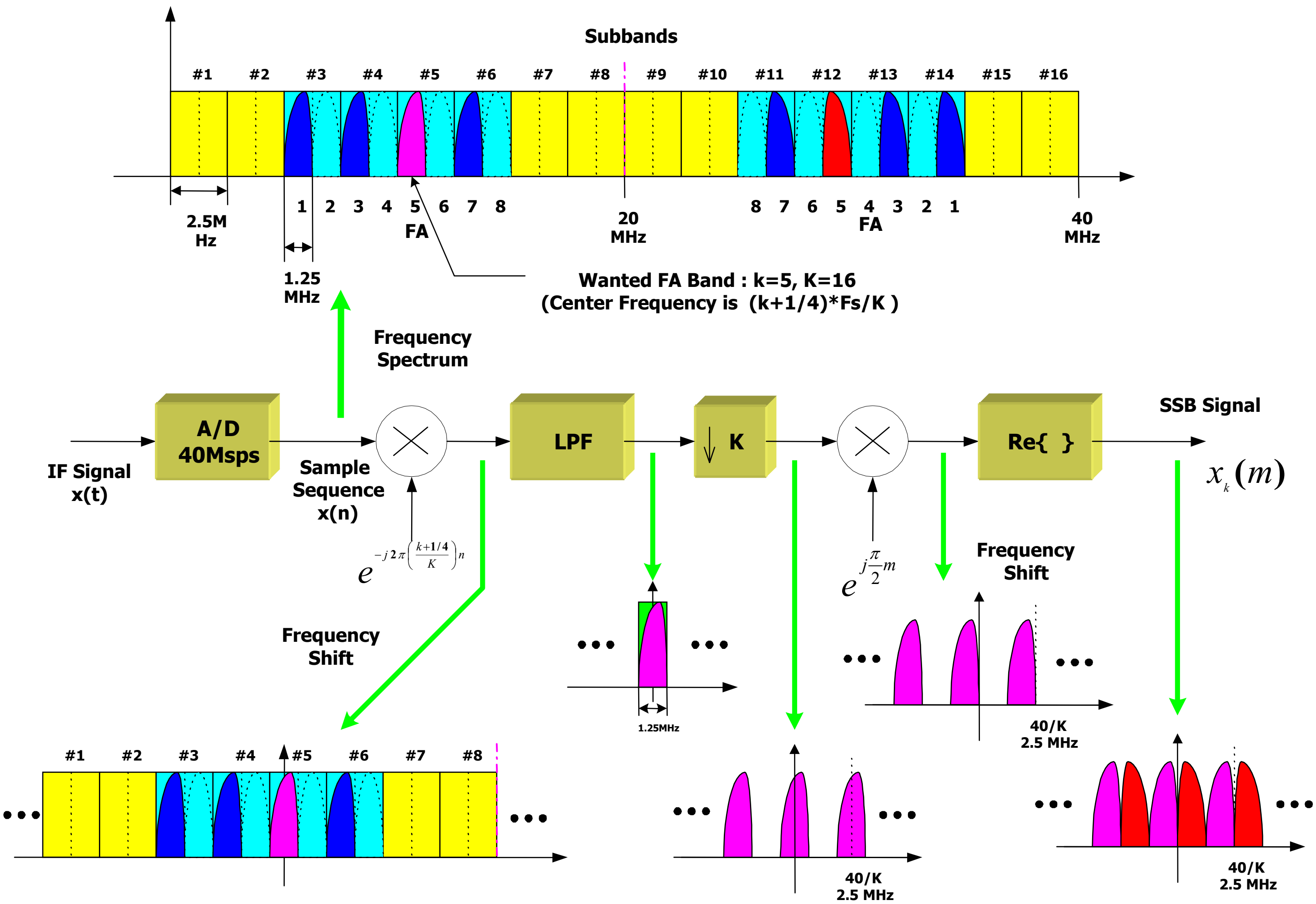


Conventional Multi-hardware Radio



Software Defined Radio

Functionality of Digital IF Channelizer



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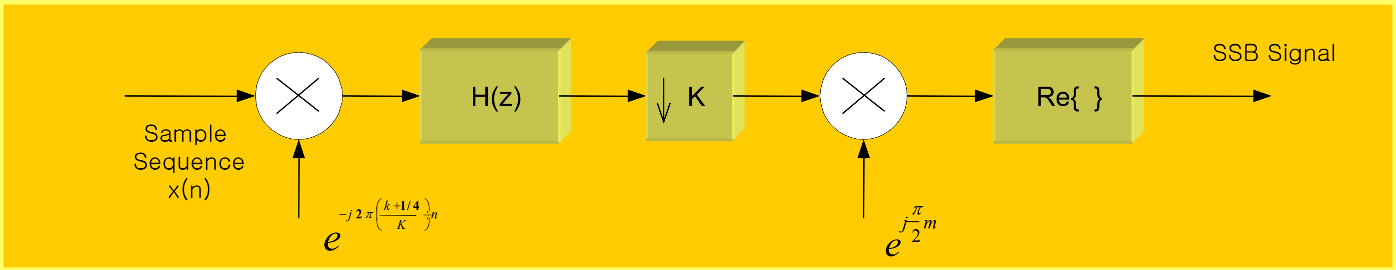
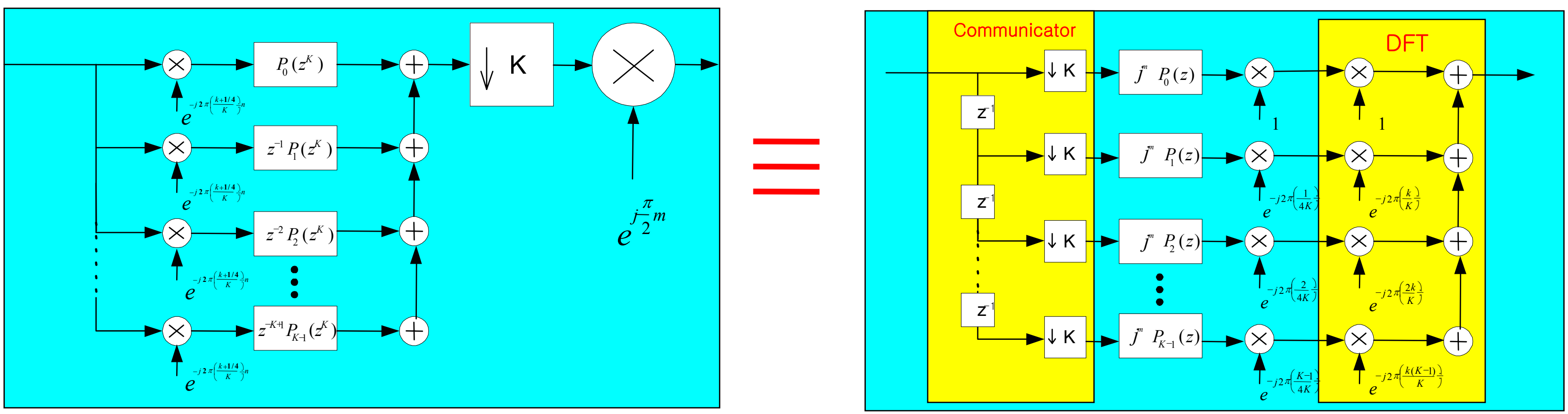
Channelizer using Polyphase Filter Bank

Prototype Lowpass Filter

$$H(z) = P_0(z^K) + z^{-1}P_1(z^K) + z^{-2}P_2(z^K) + \cdots + z^{-K+1}P_{K-1}(z^K)$$

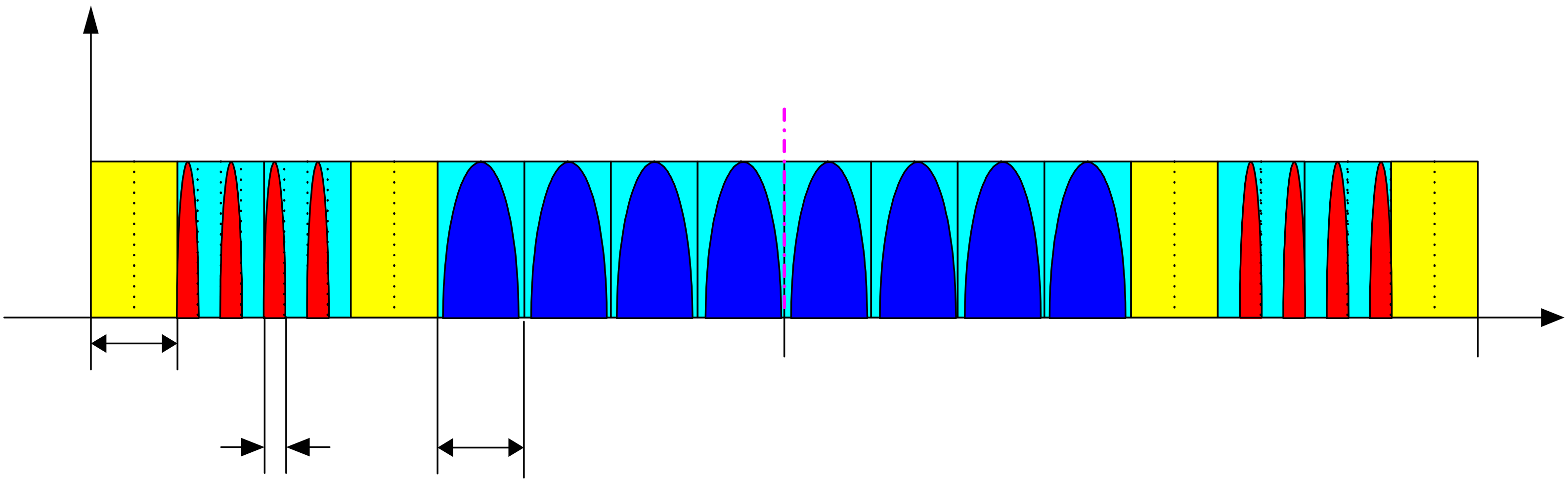




The above models are equivalent.

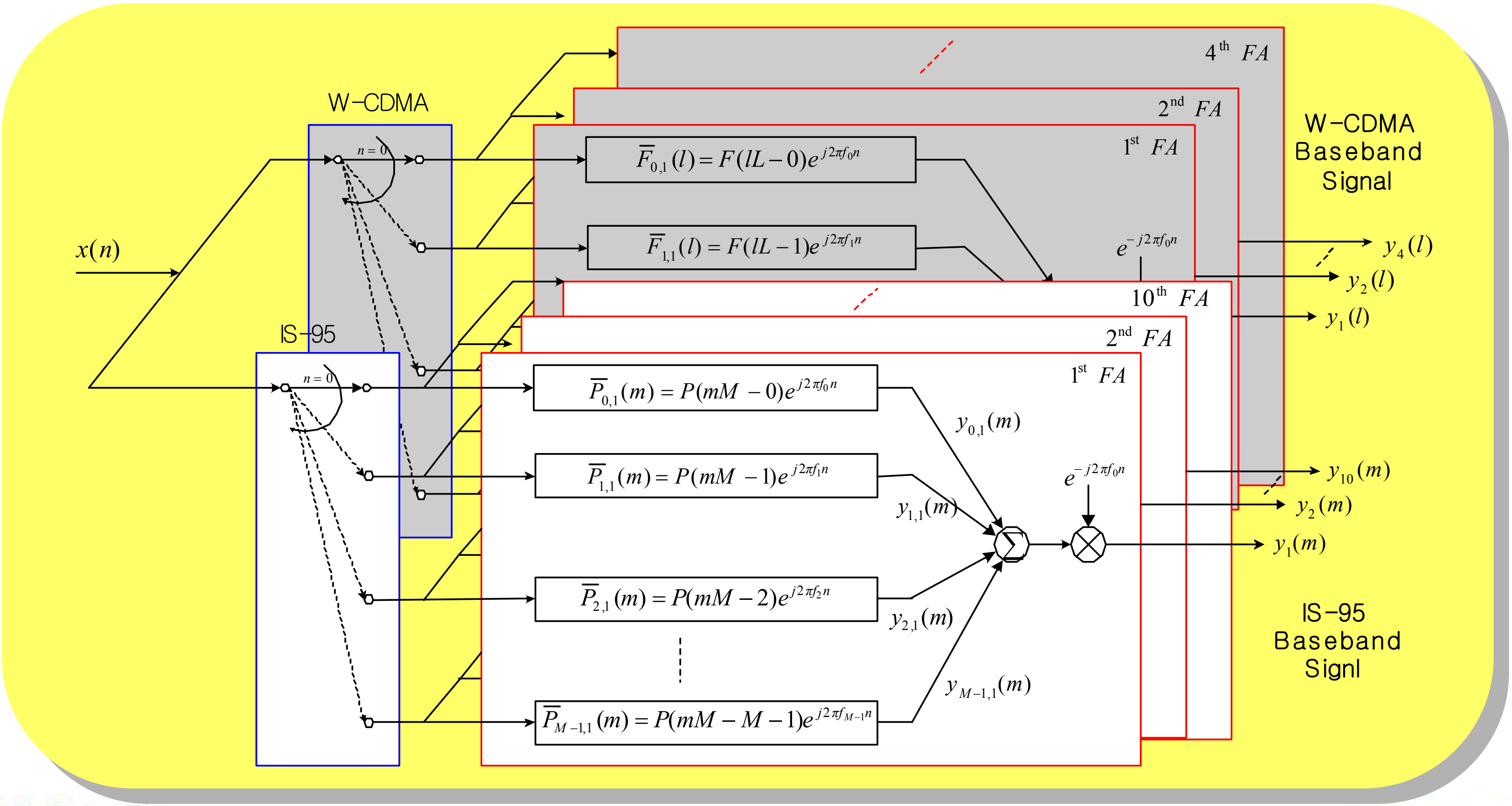
An Example : IS-95 and W-CDMA

- Sampling Frequency : 80 MHz
- FA BW : 5MHz
- IS-95 : FA BW 1.25MHz



Multiband Channelizer for IS-95 & W-CDMA

- Characteristics :
  - Polyphase filter bank structure performed with low processing clock
  - Each communicator is employed for each multi-FA standard.



Conclusions

- For future mobile communication systems, the development of multi-mode and multi-band SDR platform is necessary.
- For multi-mode and multi-band transceiver, the development of Digital IF technology is necessary.
- To realize multi-mode and multi-band SDR-based Digital IF module, reconfigurable RF devices and digital processors with high speed and low power consumption are required.
- More flexible and sophisticated digital signal processing algorithms must be employed onto SDR platform to improve the performance of future mobile communication systems.