v3.0

RadTolerant Field Programmable Gate Arrays

Features

General Characteristics

- Tested Total Ionizing Dose (TID) Survivability Level
- No Single Event Latch-up Below a Minimum LET Threshold of 80 MeV-cm2/mg for All RT Devices
- Packages: 84-Pin, 132-Pin, 172-Pin, 196-Pin, and 256-Pin Ceramic Quad Flat Pack
- Offered as E-Flow (Actel Space Level Flow) and Class B

High Density and Performance

- 4,000 to 20,000 Gates
- 2,000 to 10,000 ASIC Equivalent Gates
- Up to 85 MHz On-Chip Performance
- Up to 228 User I/Os
- Up to Four Fast, Low-Skew Clock Networks

Easy Logic Integration

- Non-Volatile, User Programmable
- Pin-Compatible Commercial Devices Available for Prototyping
- Highly Predictable Performance with 100% Automatic Place and Route
- 100% Resource Utilization with 100% Pin-Locking
- Secure Programming Technology Prevents Reverse Engineering and Design Theft
- Permanently Programmed for Instantaneous Operation on Power-Up
- Unique In-System Diagnostic and Debug Facility with Silicon Explorer
- Actel Designer Series Design Tools, Supported by Cadence, Exemplar, Mentor Graphics, Model Tech, Synopsys, Synplicity and Viewlogic Design Entry and Simulation Tools

General Description

Actel builds the most reliable field programmable gate arrays (FPGAs) in the industry, with overall antifuse reliability ratings of less than 10 failures-in-time (FITs), corresponding to a useful life of more than 40 years. Actel FPGAs are production-proven, with more than five million devices shipped and more than one trillion antifuses manufactured. Actel devices are fully tested prior to shipment, with an out-going defect level of only 122 ppm. (Further reliability data is available in the "Actel Device Reliability Report" at http://www.actel.com/products/devices/hireldev.html.)

Product Family Profile

Device	RT1020	RT1280A	RT1425A	RT1460A	RT14100A
Gates	4,000	16,000	5,000	12,000	20,000
ASIC Equivalent Gates	2,000	8,000	2,500	6,000	10,000
PLD Equivalent Gates	5,000	20,000	6,250	15,000	25,000
TTL Equivalent Package	50	200	60	150	250
20-Pin PAL Equivalent Packages	20	80	25	60	100
Logic Modules	547	1,232	310	848	1,377
S-Modules	N/A	624	160	432	697
C-Modules	547	608	150	416	680
User I/Os	69	140	100	168	228
CQFP Package Pin Count	84	172	132	196	256
Performance System Speed (Maximum)	20 MHz	40 MHz	60 MHz	60 MHz	60 MHz
Ordering Information					
Part Number (Class B)	RT1020 -CQ84B	RT1280A -CQ172B	RT1425A -CQ132B	RT1460A -CQ196B	RT14100A -CQ256B
Part Number (E-Flow)	RT1020 -CQ84E	RT1280A -CQ172E	RT1425A -CQ132E	RT1460A -CQ196E	RT14100A -CQ256E
Commercial Equivalent for Prototyping	A1020B -CQ84C	A1280A -CQ172C	A1425A -CQ132C	A1460A -CQ196C	A14100A -CQ256C

Additionally, the programmable architecture of these devices offer high performance, design flexibility, and fast and inexpensive prototyping—all without the expense of test vectors, NRE charges, long lead times, and schedule and cost penalties for design refinements.

The RT1020 device is from the A1020B design in the ACT 1 family. This device uses a combinatorial module architecture and has 2,000 ASIC equivalent gates and 69 user I/Os. The RT1020 device is fully pin- and function-capable with the commercially-equivalent A1020B-CQ84C device for easy and inexpensive Prototyping.

The RT1280A device uses the A1280A die from the ACT 2 Family of Actel FPGAs. It utilizes a two-module architecture, consisting of combinatorial modules (C-modules) and sequential modules (S-modules) optimized for both combinatorial and sequential designs. Based on Actel's patented channeled array architecture, the RT1280A has 8,000 ASIC-equivalent gates and 140 user I/Os.

The RT1280A device is fully pin- and function-compatible with the commercially-equivalent A1280A-CQ172C device for easy and inexpensive prototyping.

The RT1425A, RT1460A and RT14100A devices use the A1425A, A1460A and A14100A die, respectively. These devices are from the ACT 3 Family of Actel FPGAs, which also utilize the two-module channeled array architecture, and offer faster performance than the RT1280A. The RT1425A has 2,500 ASIC equivalent gates and 100 user I/Os, the RT1460A has 6,000 ASIC equivalent gates and 168 user I/Os, and the RT14100A has 10,000 ASIC equivalent gates and 228 user I/Os.

These devices also have fully pin- and function-compatible commercially-equivalent devices for easy and inexpensive prototyping. The A1425A-CQ132C is used for the RT1425A, the A1460A-CQ196C is used for the RT1460A, and the A14100A-CQ256C is used for the RT14100A.

Radiation Survivability

Total dose results are summarized in two ways. First, the maximum total dose level that is reached when the parts fail to meet a device specification but remain functional. For Actel FPGAs, the parameter that exceeds the specification first is ICC, the standby supply current. Second, the maximum total dose that is reached prior to the functional failure of the device.

The RT devices have varying total dose radiation survivability. The ability of these devices to survive radiation effects is both device and lot dependent. The customer must evaluate and determine the applicability of these devices to their specific design and environmental requirements.

Typical results for the RT1020 device has shown ~100 Krads (Si) for standby I_{CC} and >100 Krads for functional failure. RT1280A device have shown results from 4 to 10 Krads (Si) for standby I_{CC}, and 7 to 18 Krads for functional failure. ACT 3 devices typical results have shown 10 to 28 Krads for I_{CC}, and 20 to 77 Krads for functional failure.

Actel will provide Group E total dose testing on each lot that is available for sale. Actel will provide these reports on our website or you can contact your local sales representative to receive a copy. We will also provide a listing of available lots and devices. These results are only provided for reference and for customer information.

A summary of the radiation performance of Actel products ("Radiation Performance of Actel Products") can be found on the Actel Web site at

http://www.actel.com/products/devices/radhard/radperf.pdf

This summary will also show SEU and SEL testing that has been performed.

Disclaimer

All radiation performance information is provided for information purposes only and is not guaranteed. The total dose effects are lot-dependent, and Actel does not warrant that future devices will continue to exhibit similar radiation characteristics. In addition, actual performance can vary widely due to a variety of factors, including but not limited to, characteristics of the orbit, radiation environment, proximity to satellite exterior, amount of inherent shielding from other sources within the satellite and actual bare die variations. For these reasons, Actel does not warrant any level of radiation survivability, and it is solely the responsibility of the customer to determine whether the device will meet the requirements of the specific design.

Design Tool Support

As with all Actel FPGAs, these devices are fully supported by Actel's Designer Series development tools, which include:

- DirectTime for automated, timing-driven place and route;
- ACTgen for fast development using a wide range of macro functions; and
- ACTmap for logic synthesis.

Designer Series supports industry-leading VHDL- and Verilog-based design tools, including synthesis tools from industry leaders such as Exemplar Logic, Synplicity, and Synopsys.[1]

1. Designer Series also supports design entry and simulation tools from Cadence, Mentor Graphics, and Viewlogic.

In addition, these devices are supported by Actel's new Silicon Explorer diagnostic and debugging tool kit. Silicon Explorer dramatically reduces verification time from several hours per cycle to a few seconds by enabling real-time, in-circuit debugging. Silicon Explorer includes:

- Probe Pilot, a high-speed signal acquisition and control tool that samples data at 100 MHz (asynchronous) or 66 MHz (synchronous). Probe Pilot features 18 probing channels and connects to the user's PC via a standard serial port connection.
- Diagnostic software, which turns the PC into a fully-featured, 100 MHz logic analyzer for easy graphical analysis of waveforms.

Silicon Explorer probes 100 percent of the device circuitry using Probe Pilot's powerful, 18-channel signal acquisition capability. Individual bugs are then isolated and passed to the user interface, providing the user with complete waveform data.

RadTolerant Device Ordering Information

RT1280A – CQ 172 E

Application (Temperature Range)
- C = Commercial (0 to +70°C)
- M = Military (–55 to +125°C)
- B = MIL-STD-883 Class B
- E = Extended Flow (Space Level)

Package Lead Count

Package Type
- CQ = Ceramic Quad Flat Pack (CQFP)

Speed Grade
- Std = Standard Speed
- –1 = Approximately 15% Faster than Standard

Part Number
- RT1020 = 4,000 Gates—RadTolerant ACT 1
- RT1280A = 16,000 Gates—RadTolerant ACT 2
- RT1425A = 5,000 Gates—RadTolerant ACT 3
- RT1460A = 12,000 Gates—RadTolerant ACT 3
- RT14100A = 20,000 Gates—RadTolerant ACT 3
- A1020B = 4,000 Gates—ACT 1
- A1280A = 16,000 Gates—ACT 2
- A1425A = 5,000 Gates—ACT 3
- A1460A = 12,000 Gates—ACT 3
- A14100A = 20,000 Gates—ACT 3

Product Plan

	Application			
	C	M	B	E
ACT 2				
RT1020 Device				
84-Pin Ceramic Quad Flat Pack (CQFP)	—	—	✔	✔
A1020B Device (Prototyping Use)				
84-Pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	—
RT1280A Device				
172-Pin Ceramic Quad Flat Pack (CQFP)	—	—	✔	✔
A1280A Device (Prototyping Use)				
172-Pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	—
ACT 3				
RT1425A Device				
132-Pin Ceramic Quad Flat Pack (CQFP)	—	—	✔	✔
A1425A Device (Prototyping Use)				
132-Pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	—
RT1460A Device				
196-Pin Ceramic Quad Flat Pack (CQFP)	—	—	✔	✔
A1460A Device (Prototyping Use)				
196-Pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	—
RT14100A Device				
256-Pin Ceramic Quad Flat Pack (CQFP)	—	—	✔	✔
A14100A Device (Prototyping Use)				
172-Pin Ceramic Quad Flat Pack (CQFP)	✔	✔	✔	—

Applications: *C = Commercial*, *M = Military*, *B = MIL-STD-883 Class B*, *E = Extended Flow (Space Level)*

Availability: ✔ = *Available*, *P = Planned*, — = *Not Planned*

Device Resources

FPGA Device Type	Logic Modules	Gate Array Equivalent Gates	User I/Os				
			CQFP 84-Pin	CQFP 132-Pin	CQFP 172-Pin	CQFP 196-Pin	CQFP 256-Pin
RT1020/A1020B	547	2,000	69	—	—	—	—
RT1280A/A1280A	1,232	8,000	—	—	140	—	—
RT1425A/A1425A	310	2,500	—	100	—	—	—
RT1460A/A1460A	848	6,000	—	—	—	168	—
RT14100A/A14100A	1,377	10,000	—	—	—	—	228

Architectural Overview

The Actel architecture is composed of fine-grained logic modules which produce fast, efficient logic designs. All devices are composed of logic modules, routing resources, clock networks, and I/O modules which are the building blocks for fast logic designs.

Logic Modules

These devices contain two types of logic modules: combinatorial (C-modules) and sequential (S-modules). RT1020 and A1020B devices contain only C-modules.

The C-module, shown in Figure 1, implements the following function:

Y=!S1*!S0*D00+!S1*S0*D01+S1*!S0*D10+S1*S0*D11

where:

S0=A0*B0

S1=A1+B1

The S-module shown in Figure 2 is designed to implement high-speed sequential functions within a single logic module. The S-module implements the same combinatorial logic function as the C-module while adding a sequential element. The sequential element can be configured as either a D-type flip-flop or a transparent latch. To increase flexibility, the S-module register can be by-passed so it implements purely combinatorial logic.

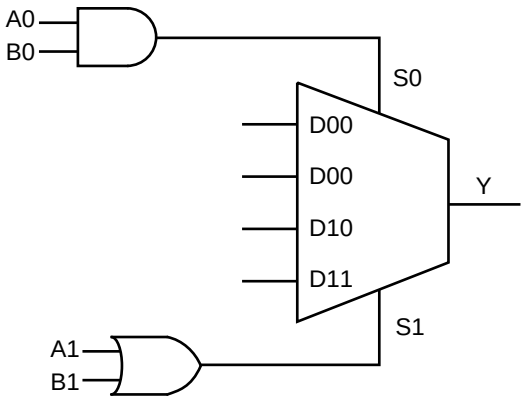


Figure 1 • *C-Module Implementation*

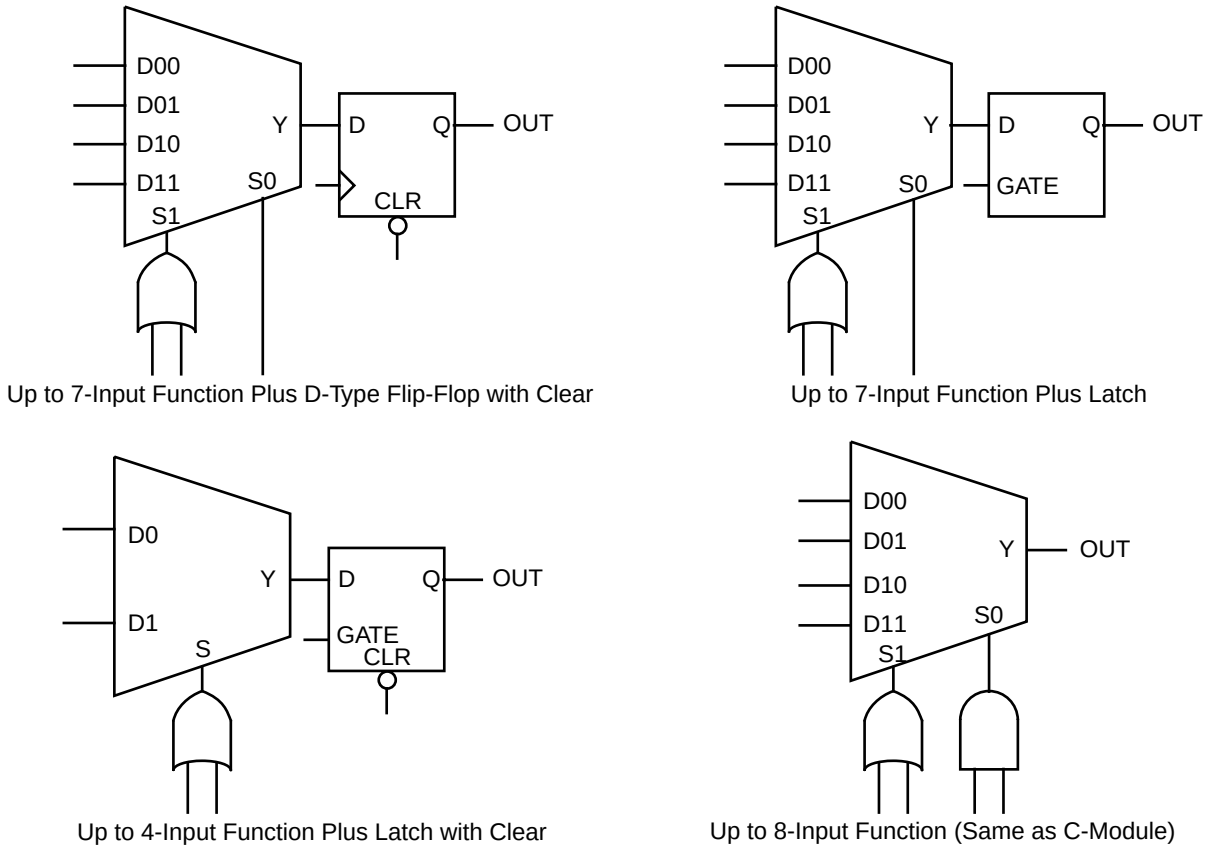


Figure 2 • *S-Module Implementation*

Flip-flops can also be created using two C-modules. The single event upset (SEU) characteristics differ between an S-module flip-flop and a flip-flop created using two C-modules. See the *Radiation Specifications* in this Data Sheet for details and the Actel Application Note, "Design Techniques for RadHard Field Programmable Gate Arrays" found at http://www.actel.com/products/radhard.html.

The ACT 1 Logic Module

The ACT 1 logic module is an 8-input, one-output logic circuit chosen for the wide range of functions it implements and for its efficient use of interconnect routing resources (Figure 3).

The logic module can implement the four basic logic functions (NAND, AND, OR, and NOR) in gates of two, three, or four inputs. Each function may have many versions, with different combinations of active-low inputs. The logic module can also implement a variety of D-latches, exclusivity functions, AND-ORs, and OR-ANDs. No dedicated hardwired latches or flip-flops are required in the array, since latches and flip-flops may be constructed from logic modules wherever needed in the application.

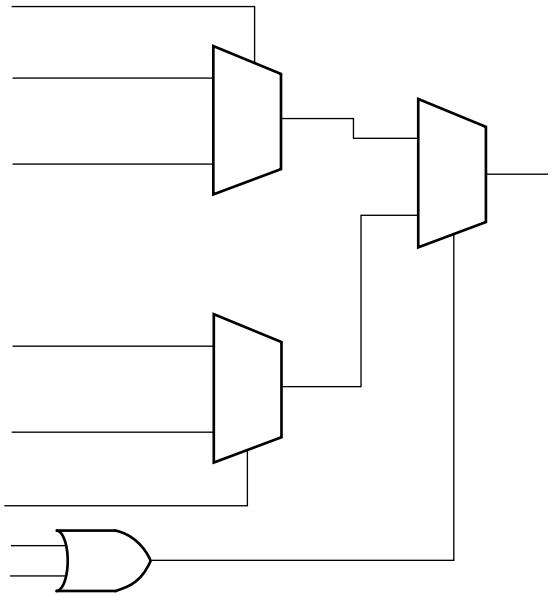
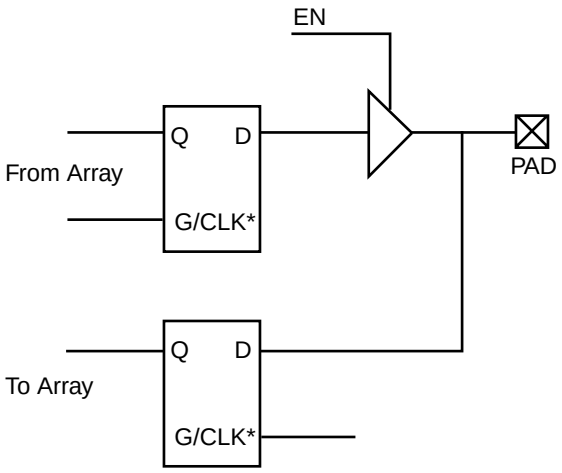


Figure 3 • *ACT 1 Logic Module*

I/O Modules

I/O modules provide the interface between the device pins and the logic array; Figure 4 is a block diagram of the I/O module. A variety of user functions, determined by a library macro selection, can be implemented in the module (refer to the Macro Library Guide for more information). I/O modules contain a tri-state buffer, and input and output latches which can be configured for input, output, or bi-directional pins (Figure 4).



* Can be Configured as a Latch or D Flip-Flop (Using C-Module)

Figure 4 • *I/O Module*

The RadHard devices contain flexible I/O structures in that each output pin has a dedicated output enable control. The I/O module can be used to latch input and/or output data, providing a fast set-up time. In addition, the Actel Designer Series software tools can build a D flip-flop, using a C-module, to register input and/or output signals.

Actel's Designer Series development tools provide a design library of I/O macros. The I/O macro library provides macro functions that can implement all I/O configurations supported by the RadHard FPGAs.

Routing Structure

The RadHard device architecture uses vertical and horizontal routing tracks to interconnect the various logic and I/O modules. These routing tracks are metal interconnects that may either be of continuous length or broken into pieces called segments. Varying segment lengths allows over 90% of the circuit interconnects to be made with only two antifuse connections. Segments can be joined together at the ends, using antifuses to increase their lengths up to the full length of the track. All interconnects can be accomplished with a maximum of four antifuses.

Horizontal Routing

Horizontal channels are located between the rows of modules, and are composed of several routing tracks. The horizontal routing tracks within the channel are divided into one or more segments. The minimum horizontal segment length is the width of a module-pair, and the maximum horizontal segment length is the full length of the channel. Any segment that spans more than one-third the row length is considered a

long horizontal segment. A typical channel is shown in Figure 5. Non-dedicated horizontal routing tracks are used to route signal nets. Dedicated routing tracks are used for the global clock networks, and for power and ground tie-off tracks.

Vertical Routing

Another set of routing tracks run vertically through the module. Vertical tracks are of three types: input, output, and long. Vertical tracks are also divided into one or more segments. Each segment in an input track is dedicated to the input of a particular module. Each segment in an output track is dedicated to the output of a particular module. Long segments are uncommitted and can be assigned during routing. Each output segment spans four channels (two above and two below), except near the top and bottom of the array where edge effects occur. LVTs contain either one or two segments. An example of vertical routing tracks and segments is shown in Figure 5.

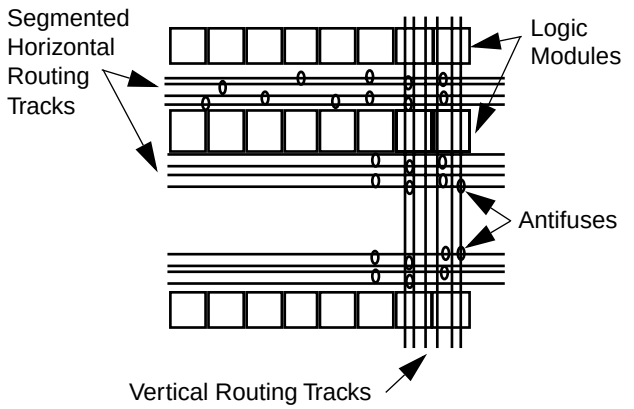


Figure 5 • *Routing Structure*

Antifuse Structures

An antifuse is a “normally open” structure as opposed to the normally closed fuse structure used in PROMs or PALs. The use of antifuses to implement a programmable logic device results in highly testable structures, as well as efficient programming algorithms. The structure is highly testable because there are no pre-existing connections; therefore, temporary connections can be made using pass transistors. These temporary connections can isolate individual antifuses to be programmed, as well as isolate individual circuit structures to be tested. This can be done both before and after programming. For example, all metal tracks can be tested for continuity and shorts between adjacent tracks, and the functionality of all logic modules can be verified.

Pin Description

CLK Clock (Input)

RT1020 and A1020B only. TTL clock input for global clock distribution networks. The clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

CLKA Clock A (Input)

Not applicable for RT1020 and A1020B. TTL clock input for global clock distribution networks. The clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

CLKB Clock B (Input)

Not applicable for RT1020 and A1020B. TTL clock input for global clock distribution networks. The clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

DCLK Diagnostic Clock (Input)

TTL clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

GND Ground

LOW supply voltage.

HCLK Dedicated (Hard-Wired) Array Clock (Input)

Not applicable for RT1020, A1020B, RT1280A and A1280A. TTL clock input for sequential modules. This input is directly wired to each S-module, offering clock speeds independent of the number of S-modules being driven. This pin can also be used as an I/O.

I/O Input/Output (Input, Output)

I/O pin functions as an input, output, tri-state, or bi-directional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are automatically driven LOW.

IOCLK Dedicated (Hard-Wired) I/O Clock (Input)

Not applicable for RT1020, A1020B, RT1280A and A1280A. TTL clock input for I/O modules. This input is directly wired to each I/O module, offering clock speeds independent of the number of I/O modules being driven. This pin can also be used as an I/O.

IOPCL Dedicated (Hard-Wired) I/O Preset/Clear (Input)

Not applicable for RT1020, A1020B, RT1280A and A1280A. TTL input for I/O preset or clear. This global input is directly wired to the preset and clear inputs of all I/O registers. This pin functions as an I/O when no I/O preset or clear macros are used.

MODE Mode (Input)

The MODE pin controls the use of diagnostic pins (DCLK, PRA, PRB, SDI). When the MODE pin is HIGH, the special functions are active. When the MODE pin is LOW, the pins function as I/Os. To provide ActionProbe capability, the MODE pin should be terminated to GND through a 10K resistor so that the MODE pin can be pulled HIGH when required.

NC No Connection

This pin is not connected to circuitry within the device.

PRA, I/O Probe A (Output)

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. PRA is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

PRB, I/O Probe B (Output)

The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when debugging has been completed. PRB is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

SDI Serial Data Input (Input)

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

V_{CC} 5V Supply Voltage

HIGH supply voltage.

Actel MIL-STD-883 Product Flow

Step	Screen	883 Method	883—Class B Requirement
1.0	Internal Visual	2010, Test Condition B	100%
2.0	Temperature Cycling	1010, Test Condition C	100%
3.0	Constant Acceleration	2001, Test Condition E (Min), Y1, Orientation Only	100%
4.0	Seal a. Fine b. Gross	1014	 100% 100%
5.0	Visual Inspection	2009	100%
6.0	Pre-Burn-In Electrical Parameters	In accordance with applicable Actel device specification	100%
7.0	Burn-in Test	1015 Condition D 160 hours @ 125°C Min.	100%
8.0	Interim (Post-Burn-In) Electrical Parameters	In accordance with applicable Actel device specification	100%
9.0	Percent Defective Allowable	5%	All Lots
10.0	Final Electrical Test	In accordance with applicable Actel device specification	
	a. Static Tests (1) 25°C (Subgroup 1, Table I, 5005) (2) –55°C and +125°C (Subgroups 2, 3, Table I, 5005)		100%
	b. Dynamic and Functional Tests (1) 25°C (Subgroup 7, Table I, 5005) (2) –55°C and +125°C (Subgroups 8A and 8B, Table I, 5005)		100%
	c. Switching Tests at 25°C (Subgroup 9, Table I, 5005)		100%
11.0	Qualification or Quality Conformance Inspection Test Sample Selection (Group A and Group B)	5005	All Lots
12.0	External Visual	2009	100%

Actel Extended Flow[1]

Step	Screen	Method	Require-ment
1.	Wafer Lot Acceptance[2]	5007 with Step Coverage Waiver	All Lots
2.	Destructive In-Line Bond Pull[3]	2011, Condition D	Sample
3.	Internal Visual	2010, Condition A	100%
4.	Serialization		100%
5.	Temperature Cycling	1010, Condition C	100%
6.	Constant Acceleration	2001, Condition E (Min), Y_1 Orientation Only	100%
7.	Visual Inspection	2009	100%
8.	Particle Impact Noise Detection	2020, Condition A	100%
9.	Radiographic	2012	100%
10.	Pre-Burn-In Test	In accordance with applicable Actel device specification	100%
11.	Burn-in Test	1015, Condition D, 240 hours @ 125°C minimum	100%
12.	Interim (Post-Burn-In) Electrical Parameters	In accordance with applicable Actel device specification	100%
13.	Reverse Bias Burn-In	1015, Condition C, 72 hours @ 150°C minimum	100%
14.	Interim (Post-Burn-In) Electrical Parameters	In accordance with applicable Actel device specification	100%
15.	Percent Defective Allowable (PDA) Calculation	5%, 3% Functional Parameters @ 25°C	All Lots
16.	Final Electrical Test	In accordance with Actel applicable device specification	100%
	a. Static Tests		100%
	(1) 25°C (Subgroup 1, Table1)	5005	
	(2) –55°C and +125°C (Subgroups 2, 3, Table 1)	5005	
	b. Dynamic and Functional Tests		100%
	(1) 25°C (Subgroup 7, Table 15)	5005	
	(2) –55°C and +125°C (Subgroups 5 and 6, 8a and b, Table 1)	5005	
	c. Switching Tests at 25°C (Subgroup 9, Table 1)	5005	100%
17.	Seal	1014	100%
	a. Fine		
	b. Gross		
18.	Qualification or Quality Conformance Inspection Test Sample Selection	5005	Group A & Group B
19	External Visual	2009	100%

Notes:

1. *Actel offers the extended flow for customers that require additional screening beyond the requirements of MIL-STD-883, Class B. Actel is compliant to the requirements of MIL-STD-883, Paragraph 1.2.1, and MIL-I-38535, Appendix A. Actel is offering this extended flow incorporating the majority of the screening procedures as outlined in Method 5004 of MIL-STD-883 Class S. The exceptions to Method 5004 are shown in notes 2 to 3 below.*
2. *Wafer lot acceptance is performed to Method 5007; however, the step coverage requirement as specified in Method 2018 must be waived.*
3. *Method 5004 requires a 100 percent, non-destructive bond pull to Method 2023. Actel substitutes a destructive bond pull to Method 2011, Condition D on a sample basis only.*

Absolute Maximum Ratings[1]

Free Air Temperature Range

Symbol	Parameter	Limits	Units
V_{CC}	DC Supply Voltage[2]	–0.5 to +7.0	V
V_I	Input Voltage	–0.5 to V_{CC} +0.5	V
V_O	Output Voltage	–0.5 to V_{CC} +0.5	V
I_{IO}	I/O Source Sink Current[5]	±20	mA
T_{STG}	Storage Temperature	–65 to +150	°C

Notes:

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the recommended operating conditions.*
2. *Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than V_{CC} + 0.5V or less than GND – 0.5V, the internal protection diode will be forward-biased and can draw excessive current.*

Recommended Operating Conditions

Parameter	Commercial	Military	Units
Temperature Range[1]	0 to +70	–55 to +125	°C
Power Supply Tolerance	±5	±10	%V_{CC}

Note:

1. *Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.*

Electrical Specifications

			Commercial		Military		
Symbol	**Parameter**	**Test Condition**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
V_{OH}[1, 2]	HIGH Level Output	I_{OH} = –4 mA (CMOS)			3.7		V
		I_{OH} = –6 mA (CMOS)	3.84				V
V_{OL}[1, 2]	LOW Level Output	I_{OL} = +6 mA (CMOS)		0.33		0.4	V
V_{IH}	HIGH Level Input	TTL Inputs	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
V_{IL}	LOW Level Input	TTL Inputs	–0.3	0.8	–0.3	0.8	V
I_{IN}	Input Leakage	V_I = V_{CC} or GND	–10	+10	–10	+10	µA
I_{OZ}	3-State Output Leakage	V_O = V_{CC} or GND	–10	+10	–10	+10	µA
C_{IO}	I/O Capacitance[3, 4]			10		10	pF
$I_{CC(S)}$	Standby V_{CC} Supply Current	V_I = V_{CC} or GND, I_O = 0 mA		2		20	mA
$I_{CC(D)}$	Dynamic V_{CC} Supply Current	See "Power Dissipation" Section					

Notes:

1. *Actel devices can drive and receive either CMOS or TTL signal levels. No assignment of I/Os as TTL or CMOS is required.*
2. *Tested one output at a time, V_{CC} = min.*
3. *Not tested; for information only.*
4. *V_{OUT} = 0V, f = 1 MHz*

Package Thermal Characteristics

The device junction to case thermal characteristic is θ_{jc}, and the junction to ambient air characteristic is θ_{ja}. The thermal characteristics for θ_{ja} are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a CQFP 172-pin package at military temperature is as follows:

$$\frac{\text{Max. junction temp. (°C)} - \text{Max. military temp.}}{\theta_{jA}\text{(°C/W)}} = \frac{150°C - 125°C}{25°C/W} = 1.0W$$

Package Type	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 300 ft/min	Units
Ceramic Quad Flat Pack	84	5	40	30	°C/W
	132	13	55	30	°C/W
	172	13	25	15	°C/W
	196	13	36	24	°C/W
	256	13	30	18	°C/W

General Power Equation

$$P = [I_{CC}\text{standby} + I_{CC}\text{active}] * V_{CC} + I_{OL} * V_{OL} * N + I_{OH} * (V_{CC} - V_{OH}) * M$$

Where:

I_{CC}standby is the current flowing when no inputs or outputs are changing.

I_{CC}active is the current flowing due to CMOS switching.

I_{OL}, I_{OH} are TTL sink/source currents.

V_{OL}, V_{OH} are TTL level output voltages.

N equals the number of outputs driving TTL loads to V_{OL}.

M equals the number of outputs driving TTL loads to V_{OH}.

An accurate determination of N and M is problematical because their values depend on the family type, on design details, and on the system I/O. The power can be divided into two components: static and active.

Static Power Component

Actel FPGAs have small static power components that result in power dissipation lower than that of PALs or PLDs. By integrating multiple PALs or PLDs into one FPGA, an even greater reduction in board-level power dissipation can be achieved.

The power due to standby current is typically a small component of the overall power. Standby power is calculated below for commercial, worst-case conditions.

I_{CC}	V_{CC}	Power
2 mA	5.25V	10.5 mW

The static power dissipated by TTL loads depends on the number of outputs driving HIGH or LOW and on the DC load current. Again, this value is typically small. For instance, a 32-bit bus sinking 4 mA at 0.33V will generate 42 mW with all outputs driving LOW, and 140 mW with all outputs driving HIGH.

Active Power Component

Power dissipation in CMOS devices is usually dominated by the active (dynamic) power dissipation. This component is frequency-dependent, a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitance due to PC board traces and load device inputs. An additional component of the active power dissipation is the totem pole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by Equation 1

$$\text{Power (uW)} = C_{EQ} * V_{CC}^2 * F \qquad (1)$$

where:

C_{EQ} is the equivalent capacitance expressed in pF.

V_{CC} is the power supply in volts (V).

F is the switching frequency in MHz.

Equivalent capacitance is calculated by measuring I_{CC}active at a specified frequency and voltage for each circuit component of interest. Measurements are made over a range of frequencies at a fixed value of V_{CC}. Equivalent capacitance is frequency-independent, so the results can be used over a wide range of operating conditions. Equivalent capacitance values are shown below.

CEQ Values for Actel FPGAs

	RT1020 A1020B	**RT1280A A1280A**	**RT1425A A1425A RT1460A A1460A RT14100A A14100A**
Modules (C_{EQM})	3.7	5.8	6.7
Input Buffers (C_{EQI})	22.1	12.9	7.2
Output Buffers (C_{EQO})	32.1	23.8	10.4
Routed Array Clock Buffer Loads (C_{EQCR})	4.6	3.9	1.6
Dedicated Clock Buffer Loads (C_{EQCD})	n/a	n/a	0.7
I/O Clock Buffer Loads (C_{EQCI})	n/a	n/a	0.9

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. Equation 2 shows a piece-wise linear summation over all components. Since the RT1280A and A1280A have two routed array clocks, the dedicated_Clk and IO_Clk terms do not apply. For all other devices all terms will apply.

$$\text{Power} = V_{CC}^2 * [(m * C_{EQM} * f_m)_{modules} + (n * C_{EQI} * f_n)_{inputs} + (p * (C_{EQO} + C_L) * f_p)_{outputs} + 0.5 * (q_1 * C_{EQCR} * f_{q1})_{routed\_Clk1} + (r_1 * f_{q1})_{routed\_Clk1} + 0.5 * (q_2 * C_{EQCR} * f_{q2})_{routed\_Clk2} + (r_2 * f_{q2})_{routed\_Clk2} + 0.5 * (s_1 * C_{EQCD} * f_{s1})_{dedicated\_Clk} + (s_2 * C_{EQCI} * f_{s2})_{IO\_Clk}] \quad (2)$$

where:

m = Number of logic modules switching at f_m

n = Number of input buffers switching at f_n

p = Number of output buffers switching at f_p

q_1 = Number of clock loads on the first routed array clock

q_2 = Number of clock loads on the second routed array clock

r_1 = Fixed capacitance due to first routed array clock

r_2 = Fixed capacitance due to second routed array clock

s_1 = Fixed number of clock loads on the dedicated array clock (Not applicable for RT1280A and A1280A.)

s_2 = Fixed number of clock loads on the dedicated I/O clock (Not applicable for RT1280A and A1280A.)

C_{EQM} = Equivalent capacitance of logic modules in pF

C_{EQI} = Equivalent capacitance of input buffers in pF

C_{EQO} = Equivalent capacitance of output buffers in pF

C_{EQCR} = Equivalent capacitance of routed array clock in pF

C_{EQCD} = Equivalent capacitance of dedicated array clock in pF

C_{EQCI} = Equivalent capacitance of dedicated I/O clock in pF

C_L = Output lead capacitance in pF

f_m = Average logic module switching rate in MHz

f_n = Average input buffer switching rate in MHz

f_p = Average output buffer switching rate in MHz

f_{q1} = Average first routed array clock rate in MHz

f_{q2} = Average second routed array clock rate in MHz

f_{s1} = Average dedicated array clock rate in MHz (Not applicable for RT1280A and A1280A.)

f_{s2} = Average dedicated I/O clock rate in MHz (Not applicable for RT1280A and A1280A.)

Fixed Capacitance Values for Actel FPGAs (pF)

Device Type	r_1 routed_Clk1	r_2 routed_Clk2
RT1020, A1020B	69	n/a
RT1280A, A1280A	168	168
RT1425A, A1425A	75	75
RT1460A, A1460A	165	165
RT14100A, A14100A	195	195

Fixed Clock Loads (s_1/s_2—ACT 3 Only)

Device Type	s_1 Clock Loads on Dedicated Array Clock	s_2 Clock Loads on Dedicated I/O Clock
RT1425A, A1425A	160	100
RT1460A, A1460A	432	168
RT14100A, A14100A	697	228

Determining Average Switching Frequency

To determine the switching frequency for a design, you must have a detailed understanding of the data input values to the circuit. The guidelines in the table below are meant to represent worst-case scenarios; they can be generally used to predict the upper limits of power dissipation.

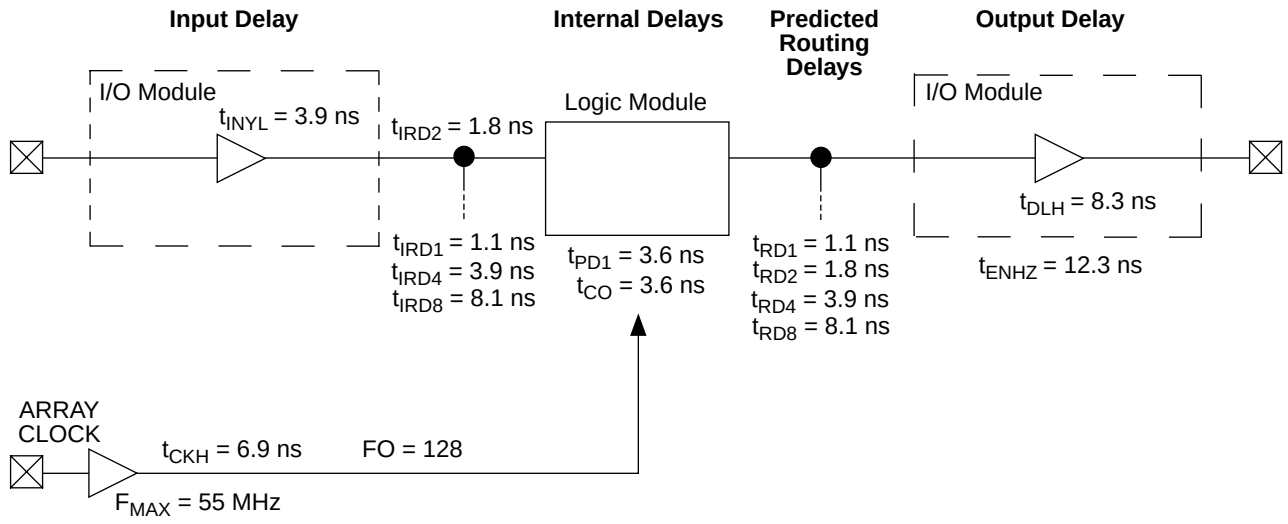
RT1020, A1020B, RT1280A, A1280A

Logic Modules (m)	=	80% of Combinatorial Modules
Input Switching (n)	=	# Inputs/4
Outputs Switching (p)	=	# Outputs/4
First Routed Array Clock Loads (q_1)	=	40% of Sequential Modules
Second Routed Array Clock Loads (q_2)	=	40% of Sequential Modules
Load Capacitance (C_L)	=	35 pF
Average Logic Module Switching Rate (f_m)	=	F/10
Average Input Switching Rate (f_n)	=	F/5
Average Output Switching Rate (f_p)	=	F/10
Average First Routed Array Clock Rate (f_{q1})	=	F
Average Second Routed Array Clock Rate (f_{q2})	=	F/2
Average Dedicated Array Clock Rate (f_{s1})	=	n/a
Average Dedicated I/O Clock Rate (f_{s2})	=	n/a

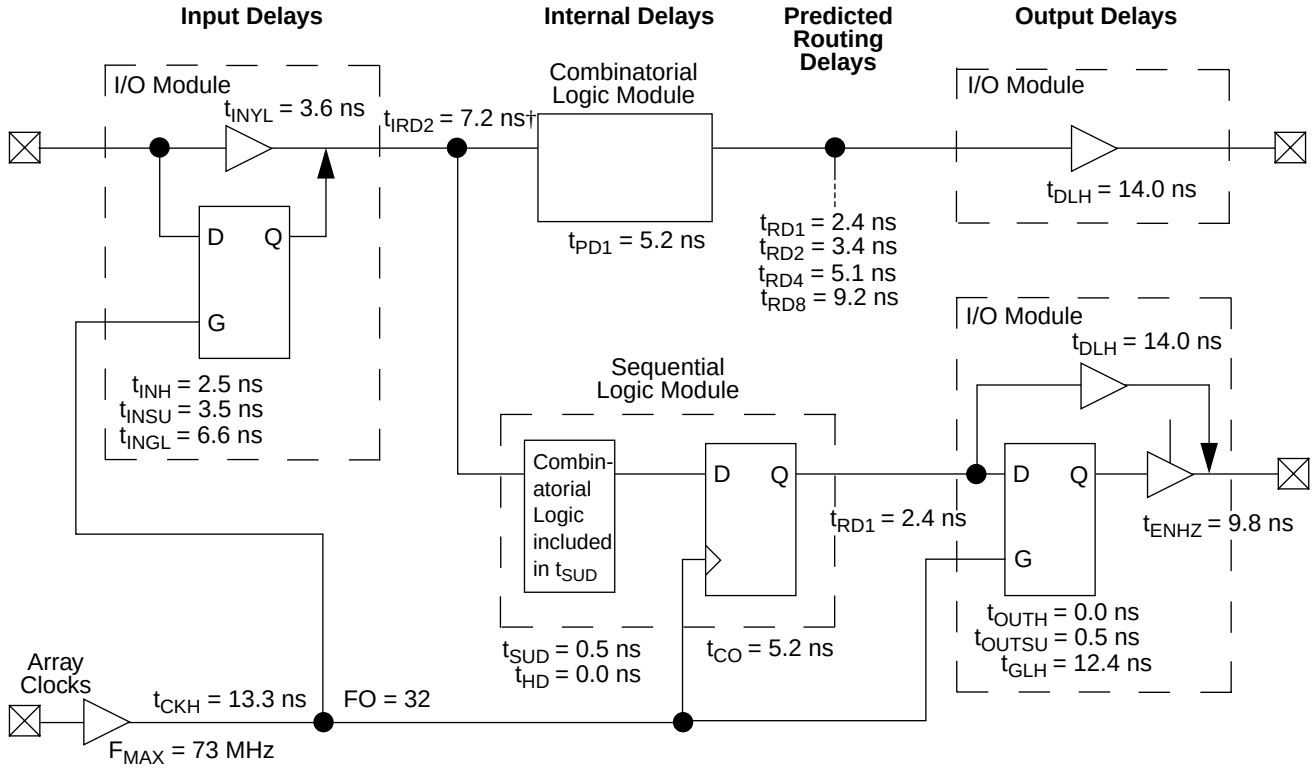
RT1425A, A1425A, RT1460A, A1460A, RT14100A, A14100A

Logic Modules (m)	=	80% of Combinatorial Modules
Input Switching (n)	=	# Inputs/4
Outputs Switching (p)	=	# Outputs/4
First Routed Array Clock Loads (q_1)	=	40% of Sequential Modules
Second Routed Array Clock Loads (q_2)	=	40% of Sequential Modules
Load Capacitance (C_L)	=	35 pF
Average Logic Module Switching Rate (f_m)	=	F/10
Average Input Switching Rate (f_n)	=	F/5
Average Output Switching Rate (f_p)	=	F/10
Average First Routed Array Clock Rate (f_{q1})	=	F/2
Average Second Routed Array Clock Rate (f_{q2})	=	F/2
Average Dedicated Array Clock Rate (f_{s1})	=	F
Average Dedicated I/O Clock Rate (f_{s2})	=	F

RT1020, A1020B Timing Module

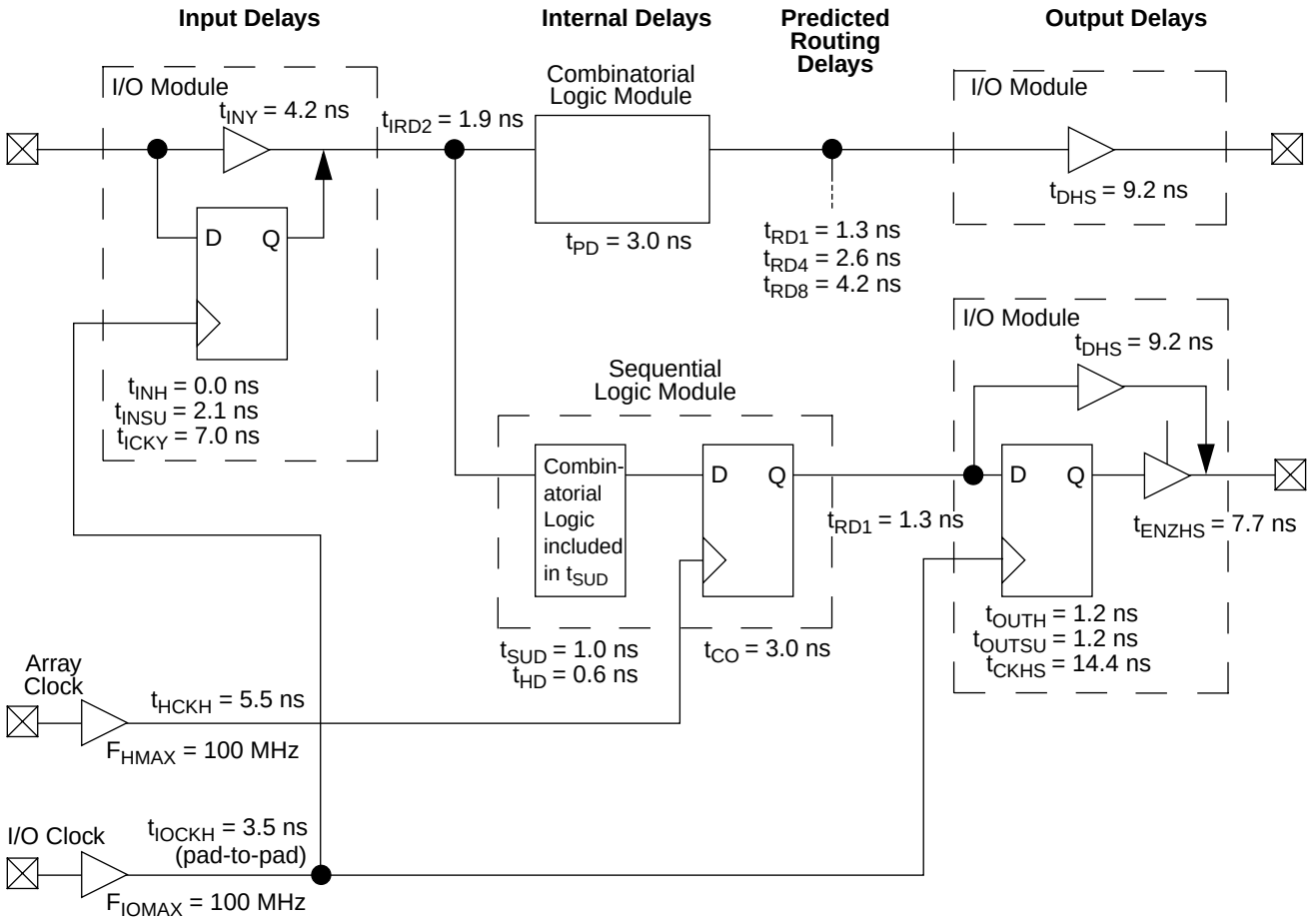


RT1280A, A1280A Timing Model*



**Values shown for RT1280A-1 at worst-case military conditions.* *† Input module predicted routing delay*

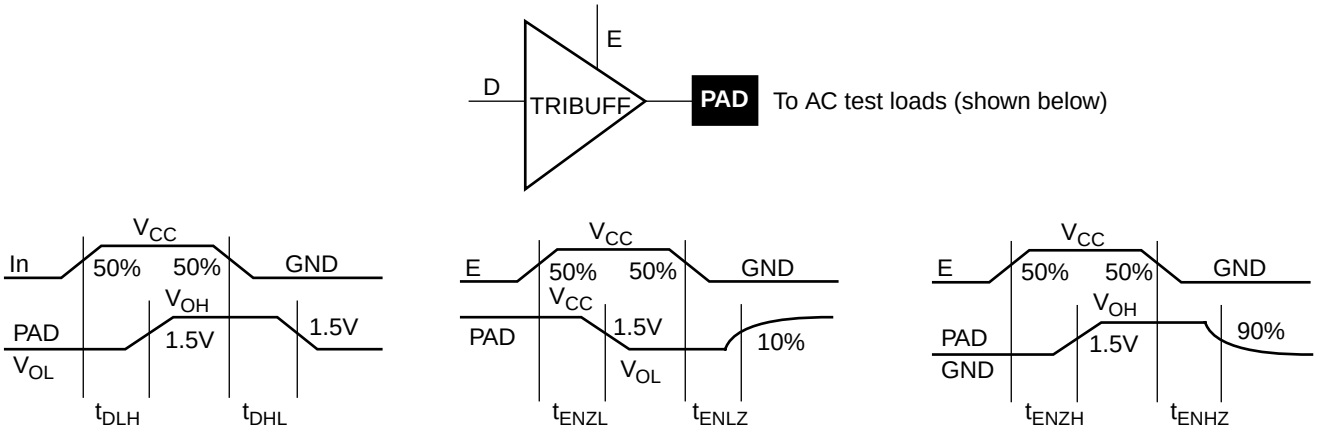
RT1425A, A1425A, RT1460A, A1460A, RT14100A, A14100A Timing Model*



**Values shown for RT14100A-1 at worst-case military conditions.*

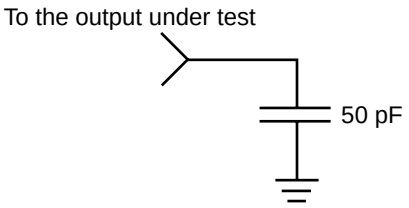
Parameter Measurement

Output Buffer Delays

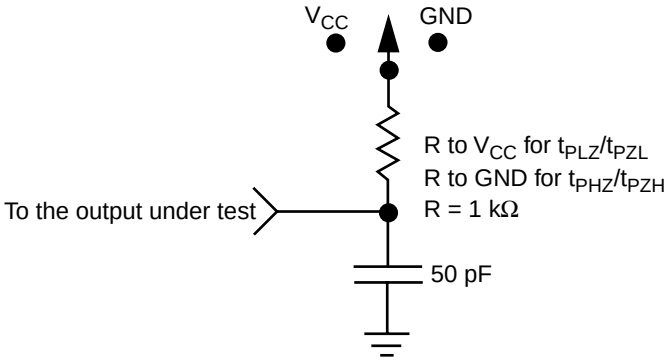


AC Test Load

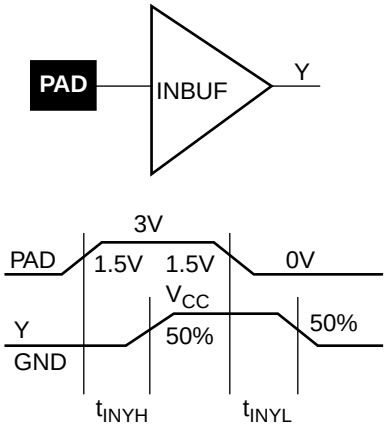
Load 1
(Used to measure propagation delay)



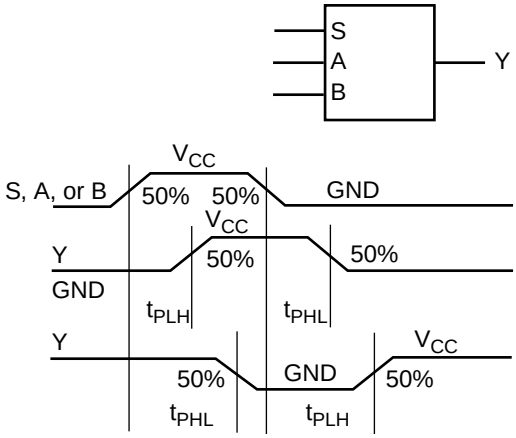
Load 2
(Used to measure rising/falling edges)



Input Buffer Delays

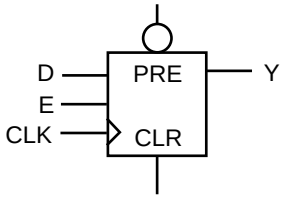


Combinatorial Macro Delays

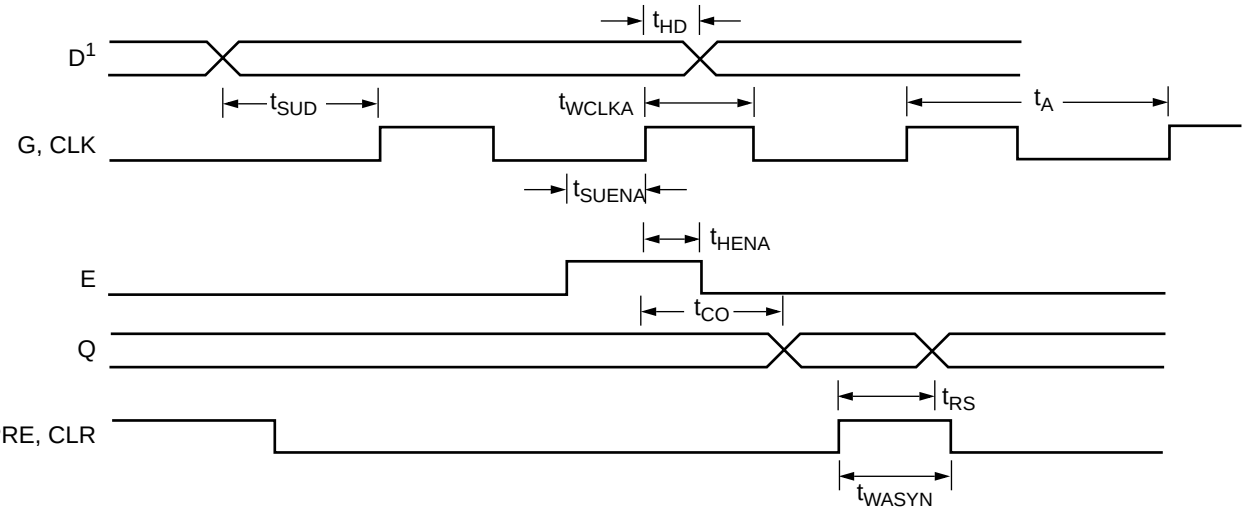


Sequential Timing Characteristics

Flip-Flops and Latches (RT1280A, A1280A)



(Positive Edge-Triggered)

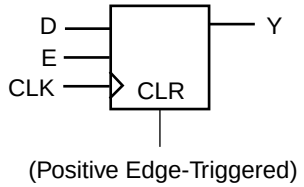


Note:

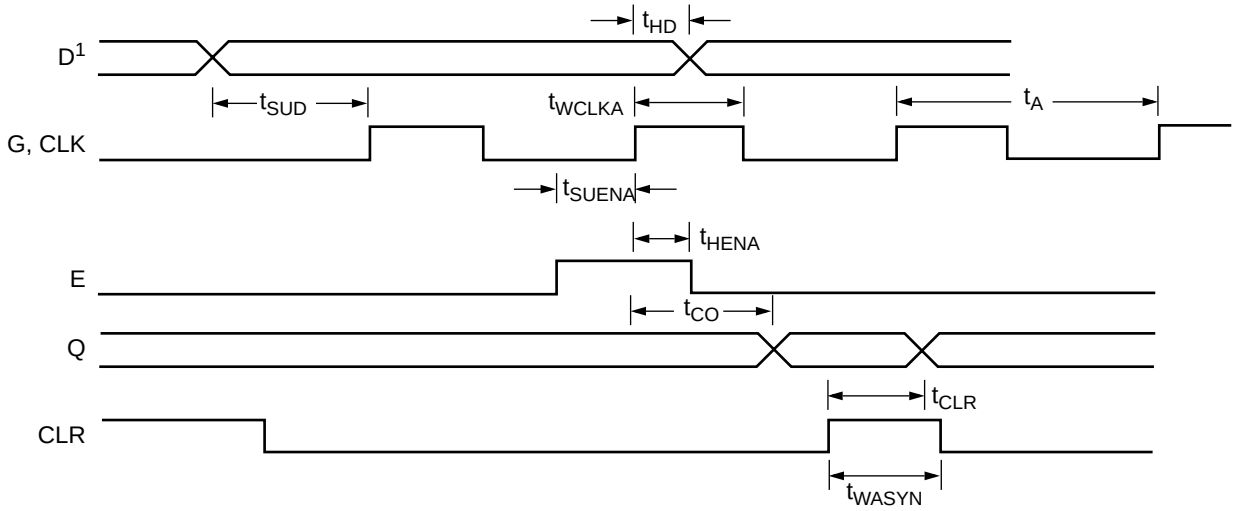
1. D represents all data functions involving A, B, and S for multiplexed flip-flops.

Sequential Timing Characteristics (continued)

Flip-Flops and Latches (RT1425A, A1425A, RT1460A, A1460A, RT14100A, A14100A)



(Positive Edge-Triggered)

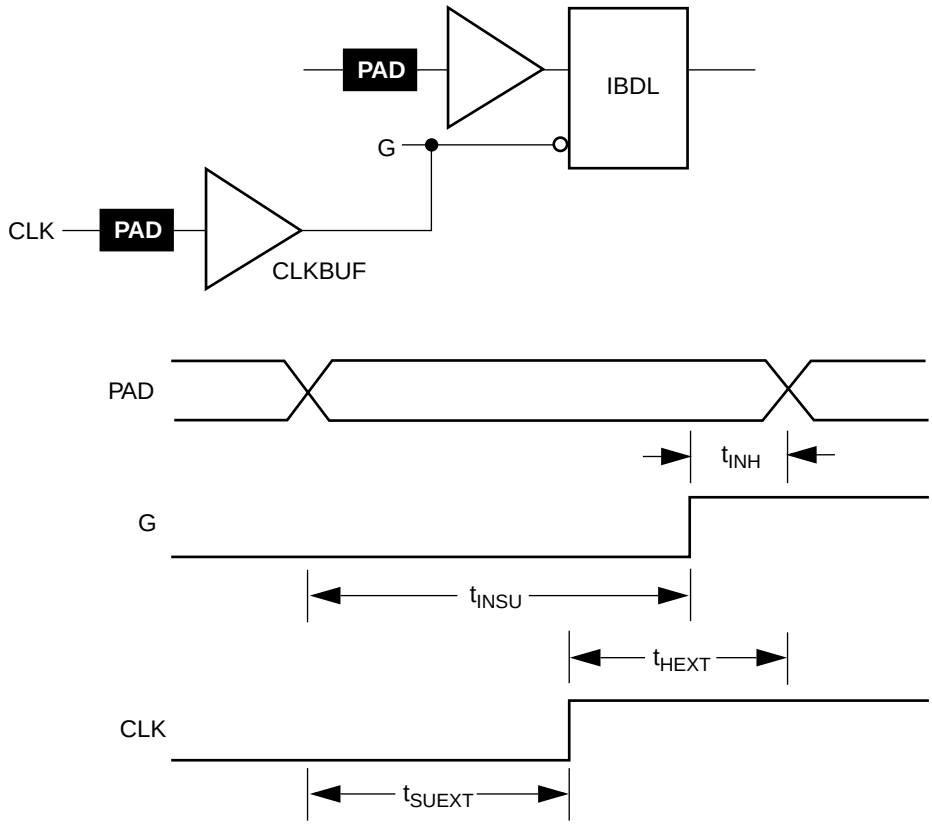


Note:

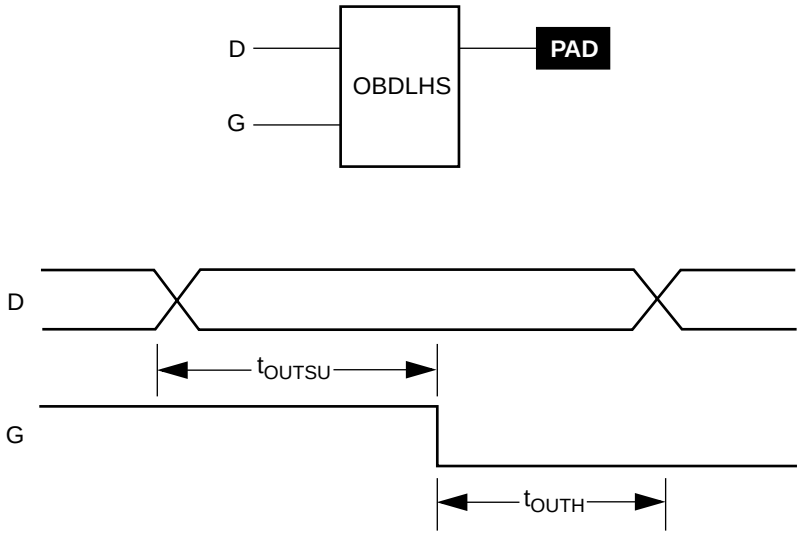
1. D represents all data functions involving A, B, and S for multiplexed flip-flops.

Sequential Timing Characteristics (continued)

Input Buffer Latches (RT1280A, A1280A)



Output Buffer Latches (RT1280A, A1280A)



RT1020, A1020B Timing Characteristics

(Worst-Case Military Conditions, V_{CC} = 4.5 V, T_J = 125°C)

Logic Module Propagation Delays				
Parameter	**Description**	**Min.**	**Max.**	**Units**
t_{PD1}	Single Module		3.6	ns
t_{PD2}	Dual Module Macros		8.4	ns
t_{CO}	Sequential Clock to Q		3.6	ns
t_{GO}	Latch G to Q		3.6	ns
t_{RS}	Flip-Flop (Latch) Reset to Q		3.6	ns
Predicted Routing Delays[1]				
t_{RD1}	FO=1 Routing Delay		1.1	ns
t_{RD2}	FO=2 Routing Delay		1.8	ns
t_{RD3}	FO=3 Routing Delay		2.6	ns
t_{RD4}	FO=4 Routing Delay		3.9	ns
t_{RD8}	FO=8 Routing Delay		8.1	ns
Sequential Timing Characteristics[2]				
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up	6.9		ns
t_{HD}[3]	Flip-Flop (Latch) Data Input Hold	0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	6.9		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	8.4		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	8.4		ns
t_A	Flip-Flop Clock Input Period	17.5		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency (FO = 128)		55	MHz

Notes:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
2. *Set-up times assume fanout of 3. Further testing information can be obtained from the DirectTime Analyzer utility.*
3. *The hold time for the DFME1A macro may be greater than 0 ns. Use the Designer Series 3.0 (or later) Timer to check the hold time for this macro.*

RT1020, A1020B Timing Characteristics (continued)

(Worst-Case Military Conditions)

Input Module Propagation Delays					
Parameter	**Description**		**Min.**	**Max.**	**Units**
t_{INYH}	Pad to Y High			3.9	ns
t_{INYL}	Pad to Y Low			3.9	ns
Input Module Predicted Routing Delays[1]					
t_{IRD1}	FO=1 Routing Delay			1.1	ns
t_{IRD2}	FO=2 Routing Delay			1.8	ns
t_{IRD3}	FO=3 Routing Delay			2.6	ns
t_{IRD4}	FO=4 Routing Delay			3.9	ns
t_{IRD8}	FO=8 Routing Delay			8.1	ns
Global Clock Network					
t_{CKH}	Input Low to High	FO = 16 FO = 128		6.0 6.9	ns
t_{CKL}	Input High to Low	FO = 16 FO = 128		7.9 8.7	ns
t_{PWH}	Minimum Pulse Width High	FO = 16 FO = 128	8.0 8.4		ns
t_{PWL}	Minimum Pulse Width Low	FO = 16 FO = 128	1.5 2.2		ns
t_{CKSW}	Maximum Skew	FO = 16 FO = 128		1.5 2.3	ns
t_P	Minimum Period	FO = 16 FO = 128	16.3 17.5		ns
f_{MAX}	Maximum Frequency	FO = 16 FO = 128		60 50	MHz

Note:

1. *These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

RT1020, A1020B Timing Characteristics (continued)

(Worst-Case Military Conditions)

Output Module Timing				
Parameter	**Description**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]				
t_{DLH}	Data to Pad High		8.3	ns
t_{DHL}	Data to Pad Low		9.3	ns
t_{ENZH}	Enable Pad Z to High		8.1	ns
t_{ENZL}	Enable Pad Z to Low		9.8	ns
t_{ENHZ}	Enable Pad High to Z		12.3	ns
t_{ENLZ}	Enable Pad Low to Z		11.1	ns
d_{TLH}	Delta Low to High		0.07	ns/pF
d_{THL}	Delta High to Low		0.10	ns/pF
CMOS Output Module Timing[1]				
t_{DLH}	Data to Pad High		9.8	ns
t_{DHL}	Data to Pad Low		7.9	ns
t_{ENZH}	Enable Pad Z to High		7.4	ns
t_{ENZL}	Enable Pad Z to Low		10.2	ns
t_{ENHZ}	Enable Pad High to Z		12.3	ns
t_{ENLZ}	Enable Pad Low to Z		11.1	ns
d_{TLH}	Delta Low to High		0.13	ns/pF
d_{THL}	Delta High to Low		0.07	ns/pF

Notes:

1. *Delays based on 35 pF loading.*
2. *SSO information can be found in the "Simultaneous Switching Output Limits for Actel FPGAs" Application Note in the 1996 Actel Data Book.*

RT1280A, A1280A Timing Characteristics

(Worst-Case Military Conditions)

Logic Module Propagation Delays[1]		'–1 Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD1}	Single Module		5.2		6.1	ns
t_{CO}	Sequential Clock-to-Q		5.2		6.1	ns
t_{GO}	Latch G-to-Q		5.2		6.1	ns
t_{RS}	Flip-Flop (Latch) Reset-to-Q		5.2		6.1	ns
Predicted Routing Delays[2]						
t_{RD1}	FO=1 Routing Delay		2.4		2.8	ns
t_{RD2}	FO=2 Routing Delay		3.4		4.0	ns
t_{RD3}	FO=3 Routing Delay		4.2		4.9	ns
t_{RD4}	FO=4 Routing Delay		5.1		6.0	ns
t_{RD8}	FO=8 Routing Delay		9.2		10.8	ns
Sequential Timing Characteristics[3, 4]						
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up	0.5		0.5		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	1.3		1.3		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	7.4		8.6		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	7.4		8.6		ns
t_{A}	Flip-Flop Clock Input Period	16.4		22.1		ns
t_{INH}	Input Buffer Latch Hold	2.5		2.5		ns
t_{INSU}	Input Buffer Latch Set-Up	3.5		3.5		ns
t_{OUTH}	Output Buffer Latch Hold	0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Set-Up	0.5		0.5		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		60		41	MHz

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Set-Up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External set-up/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal set-up (hold) time.*

RT1280A, A1280A Timing Characteristics (continued)

(Worst-Case Military Conditions)

Input Module Propagation Delays			‘–1’ Speed		‘Std’ Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INYH}	Pad-to-Y HIGH			4.0		4.7	ns
t_{INYL}	Pad-to-Y LOW			3.6		4.3	ns
t_{INGH}	G-to-Y HIGH			6.9		8.1	ns
t_{INGL}	G-to-Y LOW			6.6		7.7	ns
Input Module Predicted Routing Delays[1]							
t_{IRD1}	FO=1 Routing Delay			6.2		7.3	ns
t_{IRD2}	FO=2 Routing Delay			7.2		8.4	ns
t_{IRD3}	FO=3 Routing Delay			7.7		9.1	ns
t_{IRD4}	FO=4 Routing Delay			8.9		10.5	ns
t_{IRD8}	FO=8 Routing Delay			12.9		15.2	ns
Global Clock Network							
t_{CKH}	Input LOW to HIGH	FO = 32 FO = 384		13.3 17.9		15.7 21.1	ns
t_{CKL}	Input HIGH to LOW	FO = 32 FO = 384		13.3 18.2		15.7 21.4	ns
t_{PWH}	Minimum Pulse Width HIGH	FO = 32 FO = 384	6.9 7.9		8.1 9.3		ns
t_{PWL}	Minimum Pulse Width LOW	FO = 32 FO = 384	6.9 7.9		8.1 9.3		ns
t_{CKSW}	Maximum Skew	FO = 32 FO = 384		0.6 3.1		0.6 3.1	ns
t_{SUEXT}	Input Latch External Set-Up	FO = 32 FO = 384	0.0 0.0		0.0 0.0		ns
t_{HEXT}	Input Latch External Hold	FO = 32 FO = 384	8.6 13.8		8.6 13.8		ns
t_P	Minimum Period	FO = 32 FO = 384	13.7 16.0		16.2 18.9		ns
f_{MAX}	Maximum Frequency	FO = 32 FO = 384		73 63		62 53	MHz

Note:

1. *These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

RT1280A, A1280A Timing Characteristics (continued)

(Worst-Case Military Conditions)

Output Module Timing		‘–1 Speed		‘Std’ Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]						
t_{DLH}	Data-to-Pad HIGH		11.0		13.0	ns
t_{DHL}	Data-to-Pad LOW		13.9		16.4	ns
t_{ENZH}	Enable-to-Pad Z to HIGH		12.3		14.4	ns
t_{ENZL}	Enable-to-Pad Z to LOW		16.1		19.0	ns
t_{ENHZ}	Enable-to-Pad HIGH to Z		9.8		11.5	ns
t_{ENLZ}	Enable-to-Pad LOW to Z		11.5		13.6	ns
t_{GLH}	G-to-Pad HIGH		12.4		14.6	ns
t_{GHL}	G-to-Pad LOW		15.5		18.2	ns
d_{TLH}	Delta LOW to HIGH		0.09		0.11	ns/pF
d_{THL}	Delta HIGH to LOW		0.17		0.20	ns/pF
CMOS Output Module Timing[1]						
t_{DLH}	Data-to-Pad HIGH		14.0		16.5	ns
t_{DHL}	Data-to-Pad LOW		11.7		13.7	ns
t_{ENZH}	Enable-to-Pad Z to HIGH		12.3		14.4	ns
t_{ENZL}	Enable-to-Pad Z to LOW		16.1		19.0	ns
t_{ENHZ}	Enable-to-Pad HIGH to Z		9.8		11.5	ns
t_{ENLZ}	Enable-to-Pad LOW to Z		11.5		13.6	ns
t_{GLH}	G-to-Pad HIGH		12.4		14.6	ns
t_{GHL}	G-to-Pad LOW		15.5		18.2	ns
d_{TLH}	Delta LOW to HIGH		0.17		0.20	ns/pF
d_{THL}	Delta HIGH to LOW		0.12		0.15	ns/pF

Notes:

1. *Delays based on 50 pF loading.*
2. *SSO information can be found in the “Simultaneously Switching Output Limits for Actel FPGAs” application note.*

RT1425A, A1425A Timing Characteristics

(Worst-Case Military Conditions)

Logic Module Propagation Delays[1]		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD}	Internal Array Module		3.0		3.5	ns
t_{CO}	Sequential Clock to Q		3.0		3.5	ns
t_{CLR}	Asynchronous Clear to Q		3.0		3.5	ns
Predicted Routing Delays[2]						
t_{RD1}	FO=1 Routing Delay		1.3		1.5	ns
t_{RD2}	FO=2 Routing Delay		1.9		2.1	ns
t_{RD3}	FO=3 Routing Delay		2.1		2.5	ns
t_{RD4}	FO=4 Routing Delay		2.6		2.9	ns
t_{RD8}	FO=8 Routing Delay		4.2		4.9	ns
Logic Module Sequential Timing						
t_{SUD}	Flip-Flop (Latch) Data Input Setup	0.9		1.0		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	0.9		1.0		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	3.8		4.4		ns
t_{WCLKA}	Flip-Flop Clock Pulse Width	3.8		4.4		ns
t_A	Flip-Flop Clock Input Period	7.9		9.3		ns
f_{MAX}	Flip-Flop Clock Frequency		125		100	MHz

Notes:

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

RT1425A, A1425A Timing Characteristics (continued)

(Worst-Case Military Conditions)

I/O Module Input Propagation Delays		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INY}	Input Data Pad to Y		4.2		4.9	ns
t_{ICKY}	Input Reg IOCLK Pad to Y		7.0		8.2	ns
t_{OCKY}	Output Reg IOCLK Pad to Y		7.0		8.2	ns
t_{ICLRY}	Input Asynchronous Clear to Y		7.0		8.2	ns
t_{OCLRY}	Output Asynchronous Clear to Y		7.0		8.2	ns
Predicted Input Routing Delays[1]						
t_{IRD1}	FO=1 Routing Delay		1.3		1.5	ns
t_{IRD2}	FO=2 Routing Delay		1.9		2.1	ns
t_{IRD3}	FO=3 Routing Delay		2.1		2.5	ns
t_{IRD4}	FO=4 Routing Delay		2.6		2.9	ns
t_{IRD8}	FO=8 Routing Delay		4.2		4.9	ns
I/O Module Sequential Timing						
t_{INH}	Input F-F Data Hold (w.r.t. IOCLK Pad)	0.0		0.0		ns
t_{INSU}	Input F-F Data Setup (w.r.t. IOCLK Pad)	2.1		2.4		ns
t_{IDEH}	Input Data Enable Hold (w.r.t. IOCLK Pad)	0.0		0.0		ns
t_{IDESU}	Input Data Enable Setup (w.r.t. IOCLK Pad)	8.7		10.0		ns
t_{OUTH}	Output F-F Data Hold (w.r.t. IOCLK Pad)	1.1		1.2		ns
t_{OUTSU}	Output F-F Data Setup (w.r.t. IOCLK Pad)	1.1		1.2		ns
t_{ODEH}	Output Data Enable Hold (w.r.t. IOCLK Pad)	0.5		0.6		ns
t_{ODESU}	Output Data Enable Setup (w.r.t. IOCLK Pad)	2.0		2.4		ns

Note:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

RT1425A, A1425A Timing Characteristics (continued)

(Worst-Case Military Conditions)

I/O Module – TTL Output Timing[1]		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{DHS}	Data to Pad, High Slew		7.5		8.9	ns
t_{DLS}	Data to Pad, Low Slew		11.9		14.0	ns
t_{ENZHS}	Enable to Pad, Z to H/L, Hi Slew		6.0		7.0	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Lo Slew		10.9		12.8	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, Hi Slew		9.9		11.6	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Lo Slew		9.9		11.6	ns
t_{CKHS}	IOCLK Pad to Pad H/L, Hi Slew		10.5		11.6	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Lo Slew		15.7		17.4	ns
d_{TLHHS}	Delta Low to High, Hi Slew		0.04		0.04	ns/pF
d_{TLHLS}	Delta Low to High, Lo Slew		0.07		0.08	ns/pF
d_{THLHS}	Delta High to Low, Hi Slew		0.05		0.06	ns/pF
d_{THLLS}	Delta High to Low, Lo Slew		0.07		0.08	ns/pF
I/O Module – CMOS Output Timing[1]						
t_{DHS}	Data to Pad, High Slew		9.2		10.8	ns
t_{DLS}	Data to Pad, Low Slew		17.3		20.3	ns
t_{ENZHS}	Enable to Pad, Z to H/L, Hi Slew		7.7		9.1	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Lo Slew		13.1		15.5	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, Hi Slew		9.9		11.6	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Lo Slew		10.5		11.6	ns
t_{CKHS}	IOCLK Pad to Pad H/L, Hi Slew		12.5		13.7	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Lo Slew		18.1		20.1	ns
d_{TLHHS}	Delta Low to High, Hi Slew		0.06		0.07	ns/pF
d_{TLHLS}	Delta Low to High, Lo Slew		0.11		0.13	ns/pF
d_{THLHS}	Delta High to Low, Hi Slew		0.04		0.05	ns/pF
d_{THLLS}	Delta High to Low, Lo Slew		0.05		0.06	ns/pF

Notes:

1. *Delays based on 35 pF loading.*
2. *SSO information can be found in the "Simultaneously Switching Output Limits for Actel FPGAs" application note.*

RT1425A, A1425A Timing Characteristics (continued)

(Worst-Case Military Conditions)

Dedicated (Hard-Wired) I/O Clock Network		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{IOCKH}	Input Low to High (Pad to I/O Module Input)		3.0		3.5	ns
t_{IOPWH}	Minimum Pulse Width High	3.9		4.4		ns
t_{IOPWL}	Minimum Pulse Width Low	3.9		4.4		ns
t_{IOSAPW}	Minimum Asynchronous Pulse Width	3.9		4.4		ns
t_{IOCKSW}	Maximum Skew		0.5		0.5	ns
t_{IOP}	Minimum Period	7.9		9.3		ns
f_{IOMAX}	Maximum Frequency		125		100	MHz
Dedicated (Hard-Wired) Array Clock Network						
t_{HCKH}	Input Low to High (Pad to S-Module Input)		4.6		5.3	ns
t_{HCKL}	Input High to Low (Pad to S-Module Input)		4.6		5.3	ns
t_{HPWH}	Minimum Pulse Width High	3.9		4.4		ns
t_{HPWL}	Minimum Pulse Width Low	3.9		4.4		ns
t_{HCKSW}	Maximum Skew		0.4		0.4	ns
t_{HP}	Minimum Period	7.9		9.3		ns
f_{HMAX}	Maximum Frequency		125		100	MHz
Routed Array Clock Networks						
t_{RCKH}	Input Low to High (FO=64)		5.5		6.4	ns
t_{RCKL}	Input High to Low (FO=64)		6.0		7.0	ns
t_{RPWH}	Min. Pulse Width High (FO=64)	4.9		5.7		ns
t_{RPWL}	Min. Pulse Width Low (FO=64)	4.9		5.7		ns
t_{RCKSW}	Maximum Skew (FO=128)		1.1		1.2	ns
t_{RP}	Minimum Period (FO=64)	10.1		11.6		ns
f_{RMAX}	Maximum Frequency (FO=64)		100		85	MHz
Clock-to-Clock Skews						
$t_{IOHCKSW}$	I/O Clock to H-Clock Skew	0.0	3.0	0.0	3.0	ns
$t_{IORCKSW}$	I/O Clock to R-Clock Skew	0.0	3.0	0.0	3.0	ns
t_{HRCKSW}	H-Clock to R-Clock Skew					
	(FO = 64)	0.0	1.0	0.0	1.0	ns
	(FO = 50% max.)	0.0	3.0	0.0	3.0	ns

Note:

1. Delays based on 35 pF loading.

RT1460A, A1460A Timing Characteristics

(Worst-Case Military Conditions)

Logic Module Propagation Delays[1]		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD}	Internal Array Module		3.0		3.5	ns
t_{CO}	Sequential Clock to Q		3.0		3.5	ns
t_{CLR}	Asynchronous Clear to Q		3.0		3.5	ns
Predicted Routing Delays[2]						
t_{RD1}	FO=1 Routing Delay		1.3		1.5	ns
t_{RD2}	FO=2 Routing Delay		1.9		2.1	ns
t_{RD3}	FO=3 Routing Delay		2.1		2.5	ns
t_{RD4}	FO=4 Routing Delay		2.6		2.9	ns
t_{RD8}	FO=8 Routing Delay		4.2		4.9	ns
Logic Module Sequential Timing						
t_{SUD}	Flip-Flop (Latch) Data Input Setup	0.9		1.0		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Setup	0.9		1.0		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	4.8		5.6		ns
t_{WCLKA}	Flip-Flop Clock Pulse Width	4.8		5.6		ns
t_A	Flip-Flop Clock Input Period	9.9		11.6		ns
f_{MAX}	Flip-Flop Clock Frequency		100		85	MHz

Notes:

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

RT1460A, A1460A Timing Characteristics (continued)

(Worst-Case Military Conditions)

I/O Module Input Propagation Delays		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INY}	Input Data Pad to Y		4.2		4.9	ns
t_{ICKY}	Input Reg IOCLK Pad to Y		7.0		8.2	ns
t_{OCKY}	Output Reg IOCLK Pad to Y		7.0		8.2	ns
t_{ICLRY}	Input Asynchronous Clear to Y		7.0		8.2	ns
t_{OCLRY}	Output Asynchronous Clear to Y		7.0		8.2	ns
Predicted Input Routing Delays[1]						
t_{IRD1}	FO=1 Routing Delay		1.3		1.5	ns
t_{IRD2}	FO=2 Routing Delay		1.9		2.1	ns
t_{IRD3}	FO=3 Routing Delay		2.1		2.5	ns
t_{IRD4}	FO=4 Routing Delay		2.6		2.9	ns
t_{IRD8}	FO=8 Routing Delay		4.2		4.9	ns
I/O Module Sequential Timing						
t_{INH}	Input F-F Data Hold (w.r.t. IOCLK Pad)	0.0		0.0		ns
t_{INSU}	Input F-F Data Setup (w.r.t. IOCLK Pad)	2.1		2.4		ns
t_{IDEH}	Input Data Enable Hold (w.r.t. IOCLK Pad)	0.0		0.0		ns
t_{IDESU}	Input Data Enable Setup (w.r.t. IOCLK Pad)	8.7		10.0		ns
t_{OUTH}	Output F-F Data Hold (w.r.t. IOCLK Pad)	1.1		1.2		ns
t_{OUTSU}	Output F-F Data Setup (w.r.t. IOCLK Pad)	1.1		1.2		ns
t_{ODEH}	Output Data Enable Hold (w.r.t. IOCLK Pad)	0.5		0.6		ns
t_{ODESU}	Output Data Enable Setup (w.r.t. IOCLK Pad)	2.0		2.4		ns

Note:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

RT1460A, A1460A Timing Characteristics (continued)

(Worst-Case Military Conditions)

I/O Module – TTL Output Timing[1]		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{DHS}	Data to Pad, High Slew		7.5		8.9	ns
t_{DLS}	Data to Pad, Low Slew		11.9		14.0	ns
t_{ENZHS}	Enable to Pad, Z to H/L, Hi Slew		6.0		7.0	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Lo Slew		10.9		12.8	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, Hi Slew		11.5		13.5	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Lo Slew		10.9		12.8	ns
t_{CKHS}	IOCLK Pad to Pad H/L, Hi Slew		11.6		13.4	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Lo Slew		17.8		19.8	ns
d_{TLHHS}	Delta Low to High, Hi Slew		0.04		0.04	ns/pF
d_{TLHLS}	Delta Low to High, Lo Slew		0.07		0.08	ns/pF
d_{THLHS}	Delta High to Low, Hi Slew		0.05		0.06	ns/pF
d_{THLLS}	Delta High to Low, Lo Slew		0.07		0.08	ns/pF
I/O Module – CMOS Output Timing[1]						
t_{DHS}	Data to Pad, High Slew		9.2		10.8	ns
t_{DLS}	Data to Pad, Low Slew		17.3		20.3	ns
t_{ENZHS}	Enable to Pad, Z to H/L, Hi Slew		7.7		9.1	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Lo Slew		13.1		15.5	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, Hi Slew		10.9		12.8	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Lo Slew		10.9		12.8	ns
t_{CKHS}	IOCLK Pad to Pad H/L, Hi Slew		14.1		16.0	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Lo Slew		20.2		22.4	ns
d_{TLHHS}	Delta Low to High, Hi Slew		0.06		0.07	ns/pF
d_{TLHLS}	Delta Low to High, Lo Slew		0.11		0.13	ns/pF
d_{THLHS}	Delta High to Low, Hi Slew		0.04		0.05	ns/pF
d_{THLLS}	Delta High to Low, Lo Slew		0.05		0.06	ns/pF

Notes:

1. *Delays based on 35 pF loading.*
2. *SSO information can be found in the "Simultaneously Switching Output Limits for Actel FPGAs" application note.*

RT1460A, A1460A Timing Characteristics (continued)

(Worst-Case Military Conditions)

Dedicated (Hard-Wired) I/O Clock Network		–1 Speed		Std Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{IOCKH}	Input Low to High (Pad to I/O Module Input)		3.5		4.1	ns
t_{IOPWH}	Minimum Pulse Width High	4.8		5.7		ns
t_{IOPWL}	Minimum Pulse Width Low	4.8		5.7		ns
t_{IOSAPW}	Minimum Asynchronous Pulse Width	3.9		4.4		ns
t_{IOCKSW}	Maximum Skew		0.9		1.0	ns
t_{IOP}	Minimum Period	9.9		11.6		ns
f_{IOMAX}	Maximum Frequency		100		85	MHz
Dedicated (Hard-Wired) Array Clock Network						
t_{HCKH}	Input Low to High (Pad to S-Module Input)		5.5		6.4	ns
t_{HCKL}	Input High to Low (Pad to S-Module Input)		5.5		6.4	ns
t_{HPWH}	Minimum Pulse Width High	4.8		5.7		ns
t_{HPWL}	Minimum Pulse Width Low	4.8		5.7		ns
t_{HCKSW}	Maximum Skew		0.9		1.0	ns
t_{HP}	Minimum Period	9.9		11.6		ns
f_{HMAX}	Maximum Frequency		100		85	MHz
Routed Array Clock Networks						
t_{RCKH}	Input Low to High (FO=256)		9.0		10.5	ns
t_{RCKL}	Input High to Low (FO=256)		9.0		10.5	ns
t_{RPWH}	Min. Pulse Width High (FO=256)	6.3		7.1		ns
t_{RPWL}	Min. Pulse Width Low (FO=256)	6.3		7.1		ns
t_{RCKSW}	Maximum Skew (FO=128)		1.9		2.1	ns
t_{RP}	Minimum Period (FO=256)	12.9		14.5		ns
f_{RMAX}	Maximum Frequency (FO=256)		75		65	MHz
Clock-to-Clock Skews						
$t_{IOHCKSW}$	I/O Clock to H-Clock Skew	0.0	3.0	0.0	3.0	ns
$t_{IORCKSW}$	I/O Clock to R-Clock Skew	0.0	5.0	0.0	5.0	ns
t_{HRCKSW}	H-Clock to R-Clock Skew (FO = 64)	0.0	1.0	0.0	1.0	ns
	(FO = 50% max.)	0.0	3.0	0.0	3.0	ns

Note:

1. Delays based on 35 pF loading.

RT14100A, A14100A Timing Characteristics

(Worst-Case Military Conditions)

Logic Module Propagation Delays[1]		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD}	Internal Array Module		3.0		3.5	ns
t_{CO}	Sequential Clock-to-Q		3.0		3.5	ns
t_{CLR}	Asynchronous Clear-to-Q		3.0		3.5	ns
Predicted Routing Delays[2]						
t_{RD1}	FO=1 Routing Delay		1.3		1.5	ns
t_{RD2}	FO=2 Routing Delay		1.9		2.1	ns
t_{RD3}	FO=3 Routing Delay		2.1		2.5	ns
t_{RD4}	FO=4 Routing Delay		2.6		2.9	ns
t_{RD8}	FO=8 Routing Delay		4.2		4.9	ns
Logic Module Sequential Timing						
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up	1.0		1.0		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.6		0.6		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	1.0		1.0		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.6		0.6		ns
t_{WASYN}	Asynchronous Pulse Width	4.8		5.6		ns
t_{WCLKA}	Flip-Flop Clock Pulse Width	4.8		5.6		ns
t_A	Flip-Flop Clock Input Period	9.9		11.6		ns
f_{MAX}	Flip-Flop Clock Frequency		100		85	MHz

Notes:

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

RT14100A, A14100A Timing Characteristics (continued)

(Worst-Case Military Conditions)

I/O Module Input Propagation Delays		‘–1 Speed		‘Std’ Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INY}	Input Data Pad-to-Y		4.2		4.9	ns
t_{ICKY}	Input Reg IOCLK Pad-to-Y		7.0		8.2	ns
t_{OCKY}	Output Reg IOCLK Pad-to-Y		7.0		8.2	ns
t_{ICLRY}	Input Asynchronous Clear-to-Y		7.0		8.2	ns
t_{OCLRY}	Output Asynchronous Clear-to-Y		7.0		8.2	ns
Predicted Input Routing Delays[1]						
t_{IRD1}	FO=1 Routing Delay		1.3		1.5	ns
t_{IRD2}	FO=2 Routing Delay		1.9		2.1	ns
t_{IRD3}	FO=3 Routing Delay		2.1		2.5	ns
t_{IRD4}	FO=4 Routing Delay		2.6		2.9	ns
t_{IRD8}	FO=8 Routing Delay		4.2		4.9	ns
I/O Module Sequential Timing						
t_{INH}	Input Flip-Flop Data Hold	0.0		0.0		ns
t_{INSU}	Input Flip-Flop Data Set-Up	2.1		2.4		ns
t_{IDEH}	Input Data Enable Hold	0.0		0.0		ns
t_{IDESU}	Input Data Enable Set-Up	8.7		10.0		ns
t_{OUTH}	Output Flip-Flop Data Hold	1.2		1.2		ns
t_{OUTSU}	Output Flip-Flop Data Set-Up	1.2		1.2		ns
t_{ODEH}	Output Data Enable Hold	0.6		0.6		ns
t_{ODESU}	Output Data Enable Set-Up	2.4		2.4		ns

Note:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

RT14100A, A14100A Timing Characteristics (continued)

(Worst-Case Military Conditions)

I/O Module – TTL Output Timing[1]		‘–1 Speed		‘Std’ Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{DHS}	Data-to-Pad, High Slew		7.5		8.9	ns
t_{DLS}	Data-to-Pad, Low Slew		11.9		14.0	ns
t_{ENZHS}	Enable-to-Pad, Z to H/L, High Slew		6.0		7.0	ns
t_{ENZLS}	Enable-to-Pad, Z to H/L, Low Slew		10.9		12.8	ns
t_{ENHSZ}	Enable-to-Pad, H/L to Z, High Slew		11.9		14.0	ns
t_{ENLSZ}	Enable-to-Pad, H/L to Z, Low Slew		10.9		12.8	ns
t_{CKHS}	IOCLK Pad-to-Pad H/L, High Slew		12.2		14.0	ns
t_{CKLS}	IOCLK Pad-to-Pad H/L, Low Slew		17.8		17.8	ns
d_{TLHHS}	Delta LOW to HIGH, High Slew		0.04		0.04	ns/pF
d_{TLHLS}	Delta LOW to HIGH, Low Slew		0.07		0.08	ns/pF
d_{THLHS}	Delta HIGH to LOW, High Slew		0.05		0.06	ns/pF
d_{THLLS}	Delta HIGH to LOW, Low Slew		0.07		0.08	ns/pF
I/O Module – CMOS Output Timing[1]						
t_{DHS}	Data-to-Pad, High Slew		9.2		10.8	ns
t_{DLS}	Data-to-Pad, Low Slew		17.3		20.3	ns
t_{ENZHS}	Enable-to-Pad, Z to H/L, High Slew		7.7		9.1	ns
t_{ENZLS}	Enable-to-Pad, Z to H/L, Low Slew		13.1		15.5	ns
t_{ENHSZ}	Enable-to-Pad, H/L to Z, High Slew		11.6		14.0	ns
t_{ENLSZ}	Enable-to-Pad, H/L to Z, Low Slew		10.9		12.8	ns
t_{CKHS}	IOCLK Pad-to-Pad H/L, High Slew		14.4		16.0	ns
t_{CKLS}	IOCLK Pad-to-Pad H/L, Low Slew		20.2		22.4	ns
d_{TLHHS}	Delta LOW to HIGH, High Slew		0.06		0.07	ns/pF
d_{TLHLS}	Delta LOW to HIGH, Low Slew		0.11		0.13	ns/pF
d_{THLHS}	Delta HIGH to LOW, High Slew		0.04		0.05	ns/pF
d_{THLLS}	Delta HIGH to LOW, Low Slew		0.05		0.06	ns/pF

Notes:

1. *Delays based on 35 pF loading.*
2. *SSO information can be found in the “Simultaneously Switching Output Limits for Actel FPGAs” application note.*

RT14100A, A14100A Timing Characteristics (continued)

(Worst-Case Military Conditions)

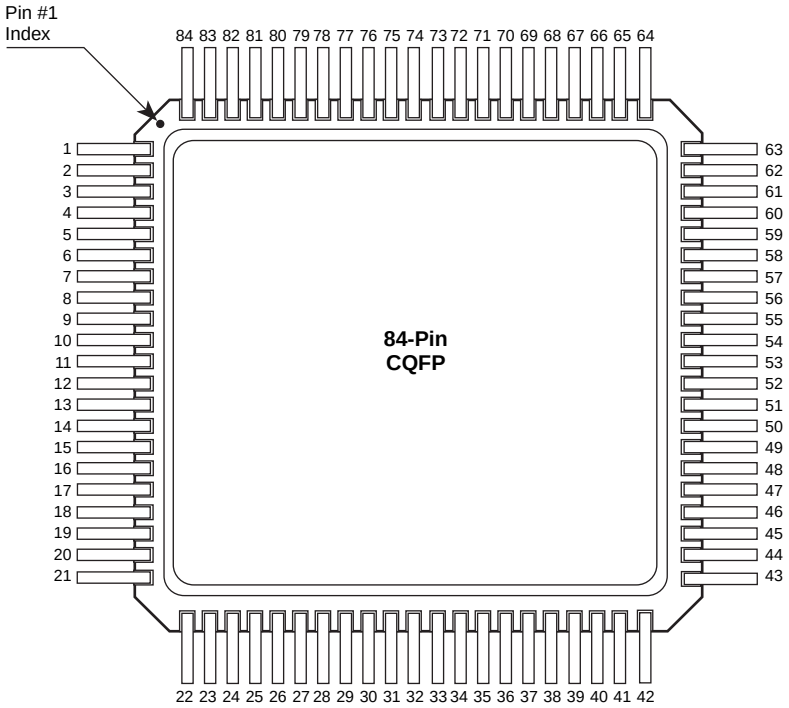
Dedicated (Hard-Wired) I/O Clock Network		‘–1’ Speed		‘Std’ Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{IOCKH}	Input LOW to HIGH (Pad to I/O Module Input)		3.5		4.1	ns
t_{IOPWH}	Minimum Pulse Width HIGH	4.8		5.7		ns
t_{IOPWL}	Minimum Pulse Width LOW	4.8		5.7		ns
t_{IOSAPW}	Minimum Asynchronous Pulse Width	3.9		4.4		ns
t_{IOCKSW}	Maximum Skew		0.9		1.0	ns
t_{IOP}	Minimum Period	9.9		11.6		ns
f_{IOMAX}	Maximum Frequency		100		85	MHz
Dedicated (Hard-Wired) Array Clock Network						
t_{HCKH}	Input LOW to HIGH (Pad to S-Module Input)		5.5		6.4	ns
t_{HCKL}	Input HIGH to LOW (Pad to S-Module Input)		5.5		6.4	ns
t_{HPWH}	Minimum Pulse Width HIGH	4.8		5.7		ns
t_{HPWL}	Minimum Pulse Width LOW	4.8		5.7		ns
t_{HCKSW}	Maximum Skew		0.9		1.0	ns
t_{HP}	Minimum Period	9.9		11.6		ns
f_{HMAX}	Maximum Frequency		100		85	MHz
Routed Array Clock Networks						
t_{RCKH}	Input LOW to HIGH (FO=256)		9.0		10.5	ns
t_{RCKL}	Input HIGH to LOW (FO=256)		9.0		10.5	ns
t_{RPWH}	Min. Pulse Width HIGH (FO=256)	6.3		7.1		ns
t_{RPWL}	Min. Pulse Width LOW (FO=256)	6.3		7.1		ns
t_{RCKSW}	Maximum Skew (FO=128)		1.9		2.1	ns
t_{RP}	Minimum Period (FO=256)	12.9		14.5		ns
f_{RMAX}	Maximum Frequency (FO=256)		75		65	MHz
Clock-to-Clock Skews						
$t_{IOHCKSW}$	I/O Clock to H-Clock Skew	0.0	3.5	0.0	3.5	ns
$t_{IORCKSW}$	I/O Clock to R-Clock Skew	0.0	5.0	0.0	5.0	ns
t_{HRCKSW}	H-Clock to R-Clock Skew (FO = 64) (FO = 50% max.)	 0.0 0.0	 1.0 3.0	 0.0 0.0	 1.0 3.0	ns

Note:

1. Delays based on 35 pF loading.

Package Pin Assignments

84-Pin CQFP (Top View)



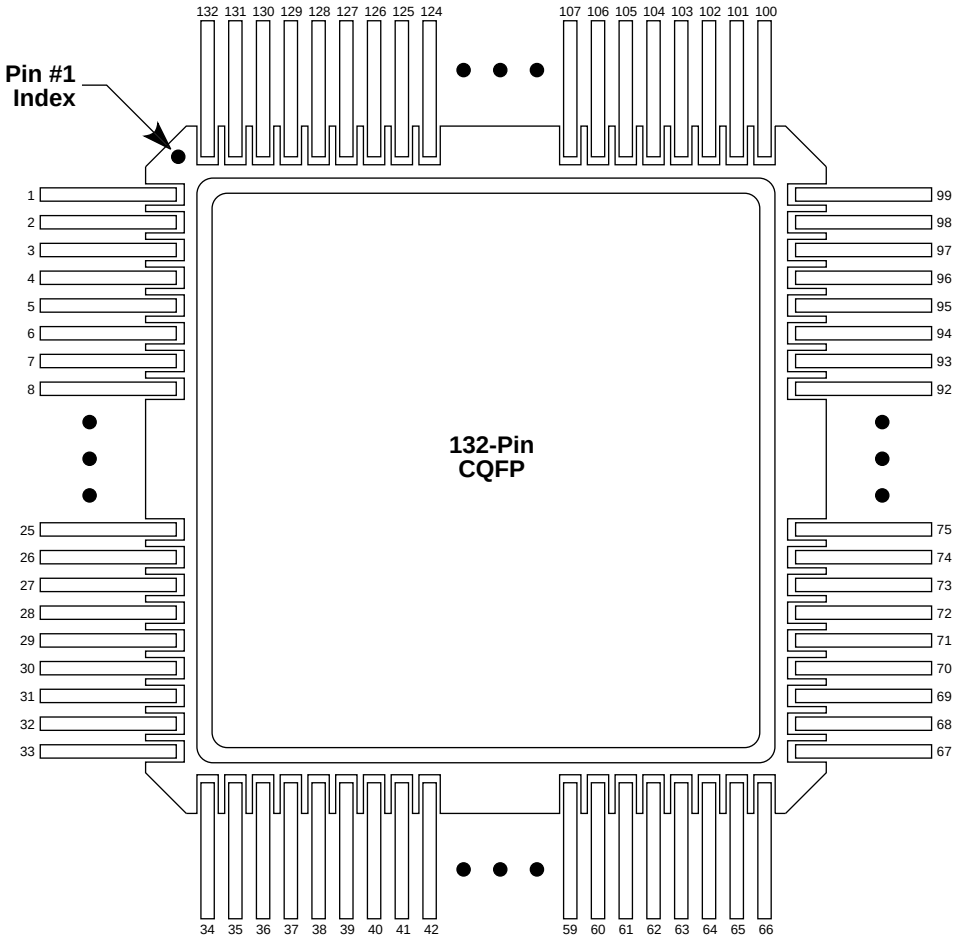
Function	RT1020, A1020B Pin Number
CLKA or I/O	53
DCLK or I/O	62
GND	7, 8, 29, 49, 50, 71
MODE	55
N/C (No Connection)	1
PRA or I/O	63
PRB or I/O	64
SDI or I/O	61
V_{CC}	14, 15, 22, 35, 56, 57, 77

Notes:

1. *MODE should be terminated to GND through a 10K resistor to enable ActionProbe usage; otherwise, it can be terminated directly to GND.*
2. *Unused I/O pins are designated as outputs by Designer and are driven LOW.*
3. *All unassigned pins are available for use as I/Os*

Package Pin Assignments (continued)

132-Pin CQFP (Top View)



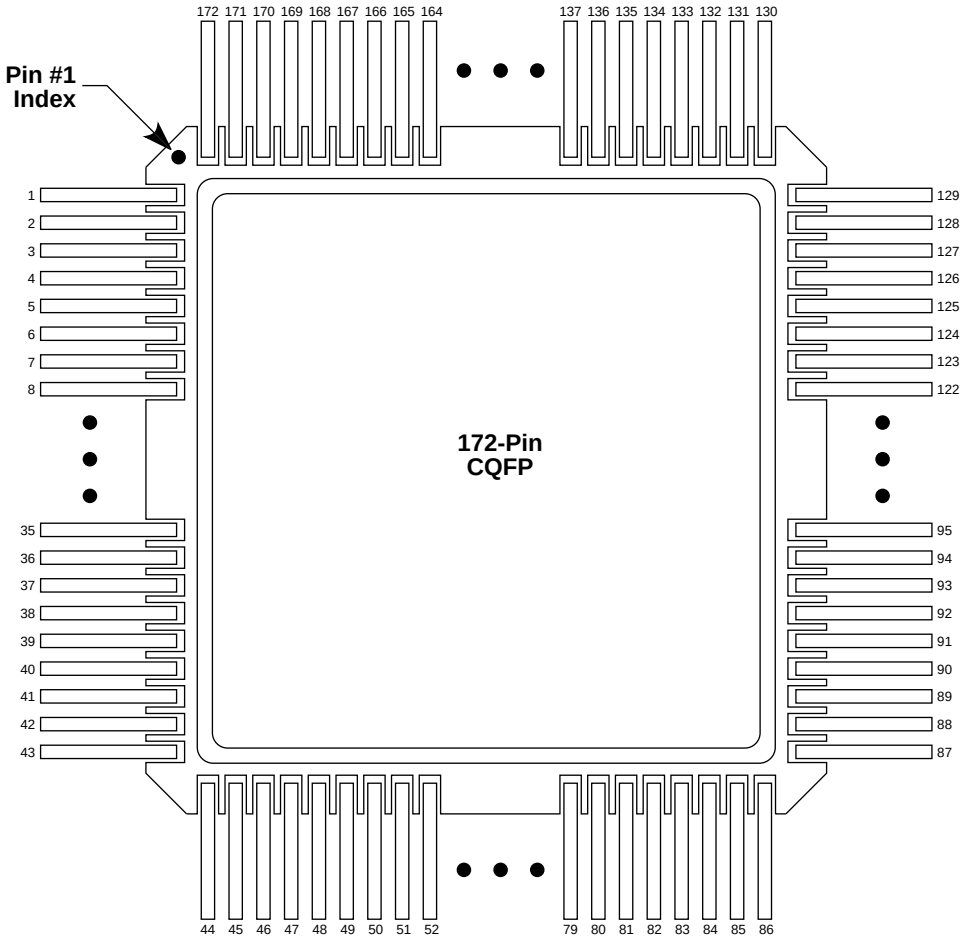
Function	RT1425A, A1425A Pin Number
CLKA or I/O	116
CLKB or I/O	117
DCLK or I/O	131
GND	2, 10, 26, 36, 42, 58, 65, 74, 90, 92, 101, 106, 122
HCLK or I/O	50
IOCLK or I/O	98
IOPCL or I/O	64
MODE	9
NC	1, 34, 66, 67, 99, 100, 132
PRA or I/O	118
PRB or I/O	48
SDI or I/O	3
V_{CC}	11, 22, 27, 43, 59, 75, 78, 89, 91, 107, 123

Notes:

1. *Unused I/O pins are designated as outputs by ALS and are driven low.*
2. *All unassigned pins are available for use as I/Os.*
3. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage, otherwise it can be terminated directly to GND.*

Package Pin Assignments (continued)

172-Pin CQFP (Top View)



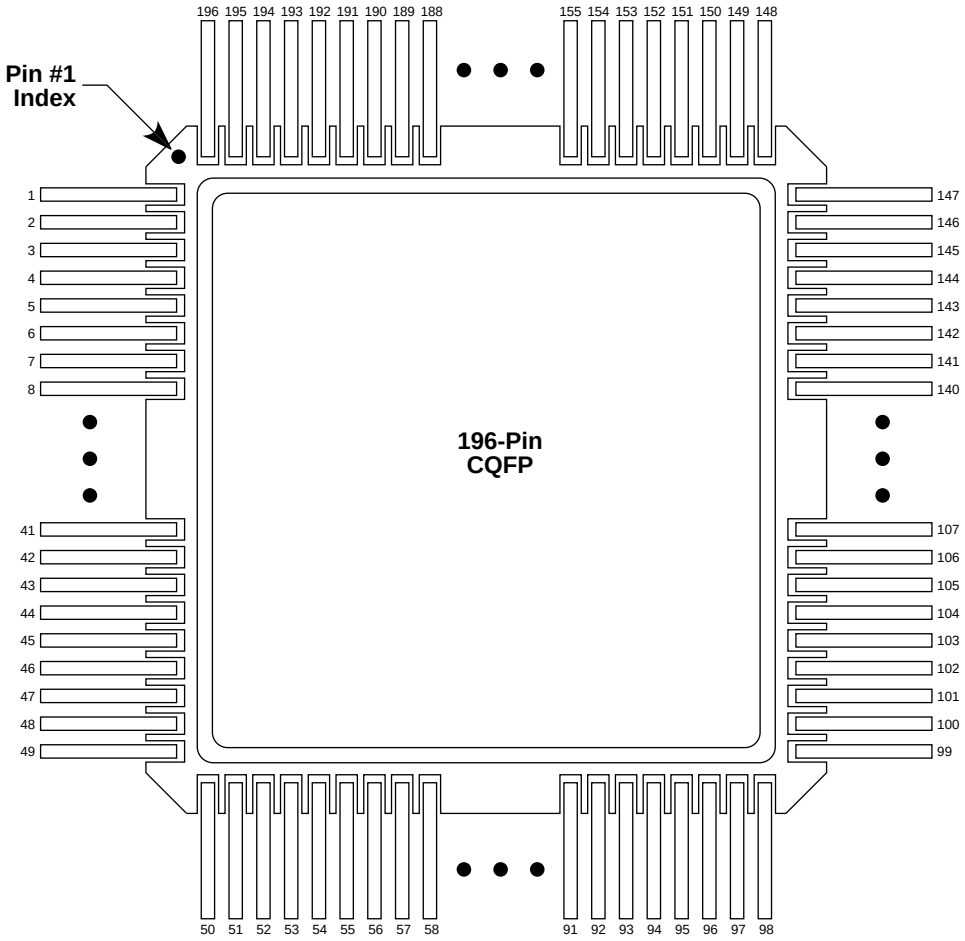
Function	RT1280A, A1280A Pin Number
CLKA or I/O	150
CLKB or I/O	154
DCLK or I/O	171
GND	7, 17, 22, 32, 37, 55, 65, 75, 98, 103, 106, 108, 118, 123, 141, 152, 161
MODE	1
PRA or I/O	148
PRB or I/O	156
SDI or I/O	131
V_{CC}	12, 23, 24, 27, 66, 80, 107, 109, 110, 113, 136, 151, 166

Notes:

1. *Unused I/O pins are designated as outputs by Designer and are driven LOW.*
2. *All unassigned pins are available for use as I/Os.*
3. *MODE should be terminated to GND through a 10K resistor to enable ActionProbe usage; otherwise, it can be terminated directly to GND.*

Package Pin Assignments (continued)

196-Pin CQFP (Top View)



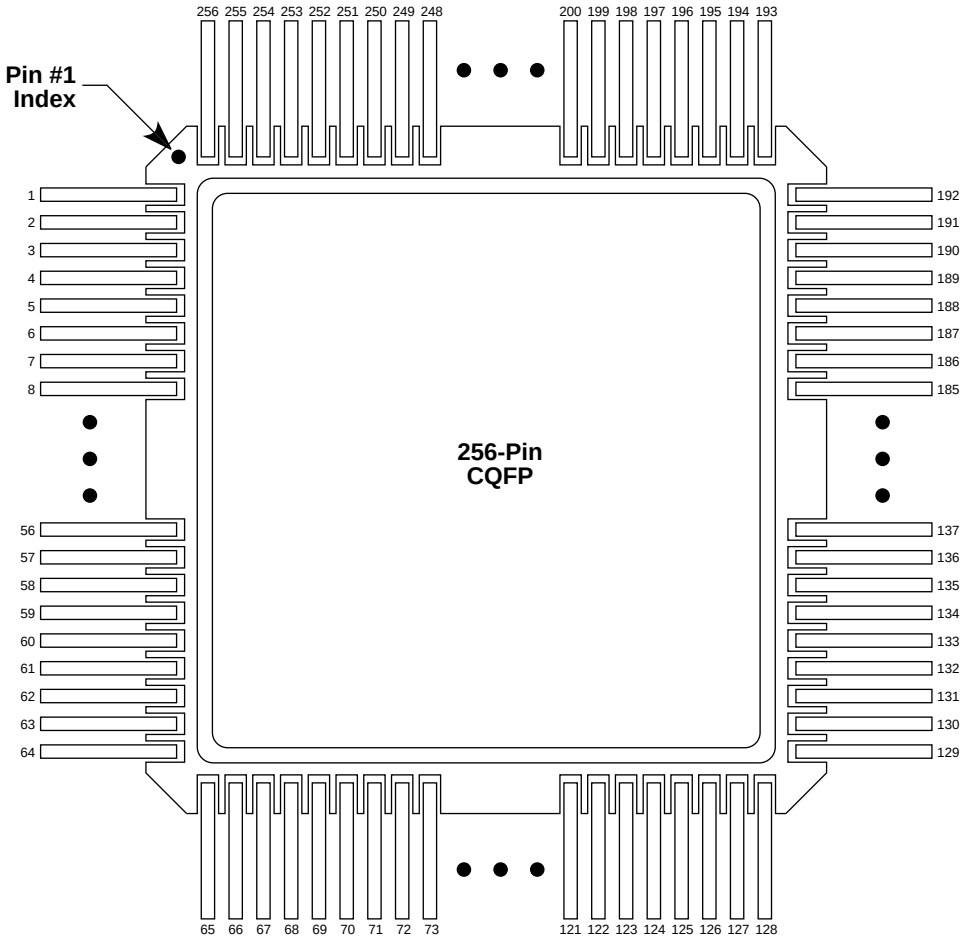
Function	RT1460A, A1460A Pin Number
CLKA or I/O	172
CLKB or I/O	173
DCLK or I/O	196
GND	1, 13, 37, 51, 52, 64, 86, 98, 101, 112, 138, 139, 149, 162, 183, 193
HCLK or I/O	77
IOCLK or I/O	148
IOPCL or I/O	100
MODE	11
PRA or I/O	174
PRB or I/O	75
SDI or I/O	2
V_{CC}	12, 38, 39, 59, 94, 110, 111, 137, 140, 155, 189

Notes:

1. *Unused I/O pins are designated as outputs by ALS and are driven low.*
2. *All unassigned pins are available for use as I/Os.*
3. *MODE should be terminated to GND through a 10K resistor to enable Actionprobe usage, otherwise it can be terminated directly to GND.*

Package Pin Assignments (continued)

256-Pin CQFP (Top View)



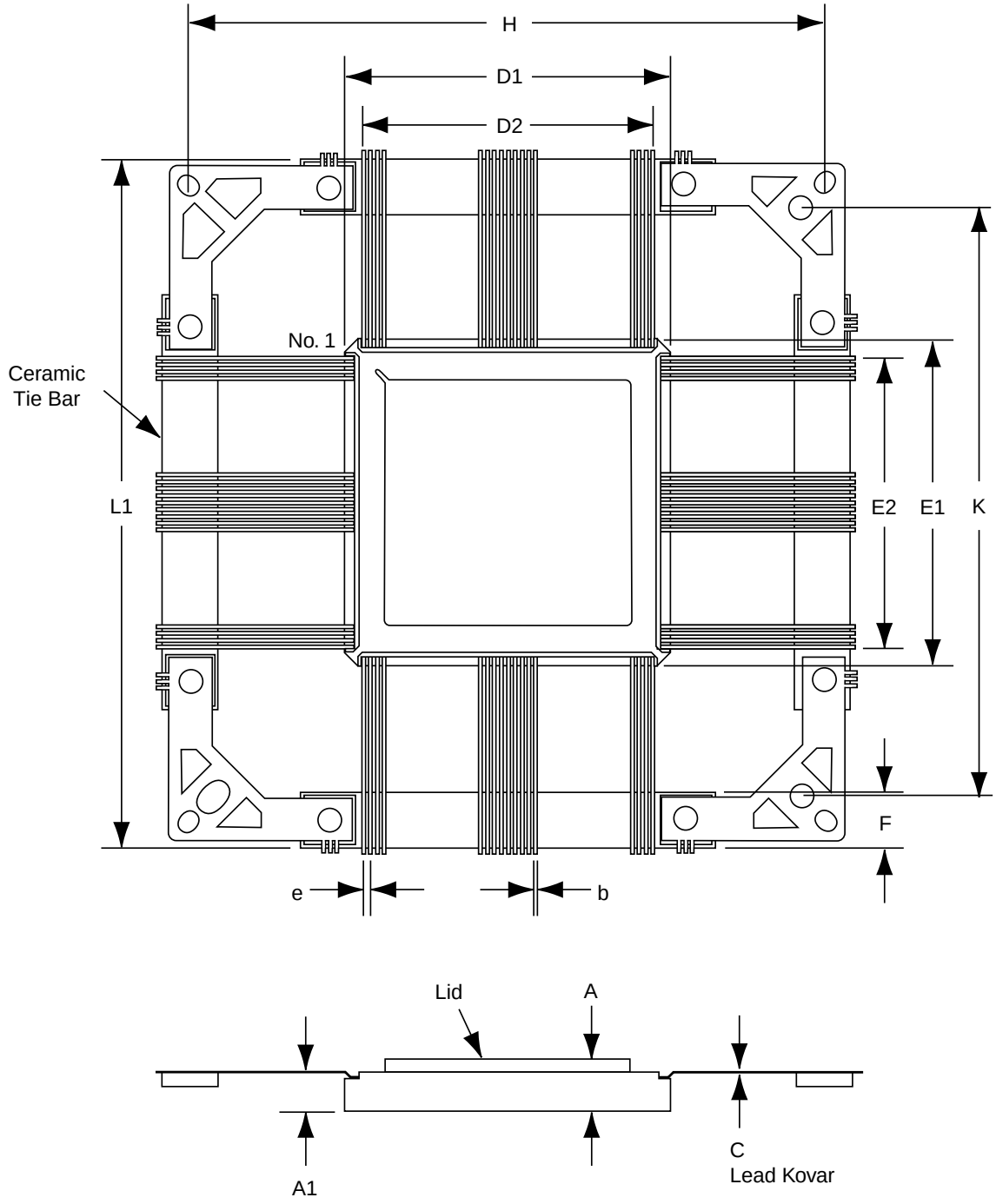
Function	RT14100A, A14100A Pin Number
CLKA or I/O	219
CLKB or I/O	220
DCLK or I/O	256
GND	1, 29, 31, 59, 91, 93, 110, 128, 158, 160, 175, 176, 189, 222, 224, 240
HCLK or I/O	96
IOCLK or I/O	188
IOPCL or I/O	127
MODE	11
PRA or I/O	225
PRB or I/O	90
SDI or I/O	2
V_{CC}	28, 30, 46, 92, 94, 141, 159, 161, 174, 221, 223

Notes:

1. *Unused I/O pins are designated as outputs by Designer and are driven LOW.*
2. *All unassigned pins are available for use as I/Os.*
3. *MODE should be terminated to GND through a 10K resistor to enable ActionProbe usage; otherwise, it can be terminated directly to GND.*

Package Mechanical Drawings

Ceramic Quad Flatpack (CQFP—Cavity Up)



Notes:

1. *All dimensions are in inches except CQ208 and CQ256 which are in millimeters.*
2. *Outside leadframe holes (from dimension H) are circular for the CQ208 and CQ256.*
3. *Seal ring and lid are connected to Ground.*
4. *Lead material is Kovar with minimum 60 miconiches gold over nickel.*
5. *Packages are shipped unformed with the ceramic tie bar.*
6. *32200DX – CQ208 has heat sink on the backside.*

Ceramic Quad Flatpack (CQFP)

	CQ84			CQ132			CQ172		
Symbol	**Min**	**Nom.**	**Max`**	**Min**	**Nom.**	**Max**	**Min**	**Nom.**	**Max**
A	0.070	0.090	0.100	0.094	0.105	0.116	0.094	0.105	0.116
A1	0.060	0.075	0.080	0.080	0.090	0.100	0.080	0.090	0.100
b	0.008	0.010	0.012	0.007	0.008	0.010	0.007	0.008	0.010
c	0.004	0.006	0.008	0.004	0.006	0.008	0.004	0.006	0.008
D1/E1	0.640	0.650	0.660	0.940	0.950	0.960	1.168	1.180	1.192
D2/E2	0.500 BSC			0.800 BSC			1.050 BSC		
e	0.025 BSC			0.025 BSC			0.025 BSC		
F	0.130	0.140	0.150	0.325	0.350	0.375	0.175	0.200	0.225
H	1.460 BSC			2.320 BSC			2.320 BSC		
K	—			2.140 BSC			2.140 BSC		
L1	1.595	1.600	1.615	2.485	2.500	2.505	2.485	2.495	2.505

Note:

1. *All dimensions are in inches except CQ256, which is in millimeters.*
2. *BSC equals Basic Spacing between Centers. This is a theoretical true position dimension and so has no tolerance.*

Ceramic Quad Flatpack (CQFP)

	CQ196			CQ256		
Symbol	**Min**	**Nom.**	**Max**	**Min**	**Nom.**	**Max**
A	0.094	0.105	0.116	2.28	2.67	3.06
A1	0.080	0.090	0.100	1.93	2.29	2.65
b	0.007	0.008	0.010	0.18	0.20	0.22
c	0.004	0.006	0.008	0.11	0.15	0.18
D1/E1	1.336	1.350	1.364	35.64	36.00	36.36
D2/E2	1.200 BSC			31.5 BSC		
e	0.025 BSC			0.50 BSC		
F	0.175	0.200	0.225	7.05	7.75	8.45
H	2.320 BSC			70.00 BSC		
K	2.140 BSC			65.90 BSC		
L1	2.485	2.495	2.505	74.60	75.00	75.40

Note:

1. *All dimensions are in inches except CQ256, which is in millimeters.*
2. *BSC equals Basic Spacing between Centers. This is a theoretical true position dimension and so has no tolerance.*

http://www.actel.com

Actel Europe Ltd.
Daneshill House, Lutyens Close
Basingstoke, Hampshire RG24 8AG
United Kingdom
Tel: +44.(0)1256.305600
Fax: +44.(0)1256.355420

Actel Corporation
955 East Arques Avenue
Sunnyvale, California 94086
USA
Tel: 408.739.1010
Fax: 408.739.1540

Actel Japan
EXOS Ebisu Bldg. 4F
1-24-14 Ebisu Shibuya-ka
Tokyo 150 Japan
Tel: +81.(0)3.3445.7671
Fax: +81.(0)3.3445.7668

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