Test Vector Guidelines

This application note provides guidelines for test vector sets. These guidelines are used in functional verification of designs in Actel FPGAs. A standardized format helps customers and Actel in the following ways:

- Improves simulation by reducing errors
- Simplifies design verification on automatic test equipment
- Reduces project cycle times
- Reduces debugging costs

This document will provide guidelines in several aspects of design verification, including:

- Waveform file formats
- Timing and sampling
- Tester constraints
- Handling bidirectional signals
- Simultaneously-switching outputs (SSOs)

Vector File Formats

The vector files should be ASCII files in a tabular format. The table should contain only binary signals. ALL external signals MUST be included in the file. Additionally, controls must be included in the file. These can be external (provide bidirectional signals) or internal. Either internal or external for bidirectional signals MUST also be included in the file. Each line in the file must be associated with a time that is increasing uniformly with each simulation cycle. There are two possibilities. First, a non-return-to-zero (NRZ) format can be used. This implies two lines in the file associated with each cycle. The other option is to use either a return-to-zero (RZ) or a return-to-one (RTO) format. In these cases there is a single line per cycle. The format cannot be changed within a given vector file for any signal.

Individual entries in each line should use the following guidelines:

- Inputs – '0', '1', 'Z', or 'X'
- Outputs – 'L', 'H', 'Z', or 'X'
- Bidirectionals
  - When used as an input – '0', '1', 'Z', or 'X'
  - When used as an output – 'L', 'H', 'Z', or 'X'

Since signal entries in existing customer files may not conform to the above guidelines, Actel can provide routines to automatically translate ASCII vector files.

A sample of a vector file in NRZ format is given in Figure 1 on page 2.

Tester Constraints

Timing and Sampling

Synchronous vector files are ALWAYS required– even for asynchronous designs. A key issue is the stimulation and sampling of signals in the vector file. Figure 2 on page 2 illustrates a simple logic network with a clock, an input signal, and an output signal. The output signal shown changes as a result of a change in the input signal. This change is reflected after the next (positive) edge of the clock in the circuit shown. The assertion of IN must be far enough in advance of the rising edge of the CLK signal to allow the signal to propagate through the input combinatorial logic and also meet the data input's setup requirements relative to the clock edge. In addition, there is a tester-specific requirement. The test equipment has pin-to-pin skew in the order of a few nanoseconds, and accounting for this skew is difficult in simulations. After the flip-flop, as shown in Figure 2 on page 2, there may also be combinatorial logic. The sampling of an output (for comparison with its expected value in a vector file) must be done after the value has had time to settle.

Figure 3 on page 2 shows the relative timing of the CLK, IN, and OUT signals. The time t_A corresponds to the minimum recommended assertion time of IN before the rising edge of CLK. Similarly, t_B is the minimum time after the rising edge of CLK when the OUT signal can be accurately sampled. The value of t_A should be at least 7 ns in fast parts like Actel's SX/SX-A family and at least 10 ns in slower families. The value of t_B should be at least 10 ns in all parts. Also avoid problems with tester pin-to-pin skew (an output sampled when an input for the NEXT cycle is asserted), the assertion and sampling points should be 5 ns or more apart.

An additional timing constraint is imposed by bidirectional signals. Contention occurs when the tester switches to drive a pin as an output *while the same pin is already acting as a driver*. Avoiding contention is important, since the tester is unable to both drive and not drive on a given cycle. The bidirectional control signals should be adjusted so that I/O drive direction changes occur just before (or at) the cycle boundary under worst-case speed conditions.

```
                    Bidir
   Clock     Inputs Control  Bidirectionals                    Outputs

     0  XXXXXXXXXXXXXXXXX  XXXXXXXXXXXXXXXX  XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
    15  XXXXXXXXXXXXXXXX   XXXXXXXXXXXXXXXX  XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
    30  X101111011111110011  1111111111111111  LXLLLLXXLXXLHXHHLXXXXHHHHHXHXHHHHLHXHHXHH
    45  1101111011111110011  1111111111111111  LXLLLLXXLXXLHXHHLXXXXHHHHHXHXHHHHLHXHHXHH
    60  0101111111111111011  1100000001111111  LXLLLLXXLXXHXHHHLXXXXHHHHHXHXHHHLHXHHHXHH
    75  1101111111111111011  1110000001111111  LHLLLLXHLXXHXHHHLXXXXHHHHHXHXHHHHLHHHHXHH
    90  0101111111111111011  1111111111111111  LHLLLLXHLXXHXHHHLXXXXHHHHHXHXHHHHLHHHHXHH
   105  1101111111111111011  0HHHHHHHHHHHHHHH  LHLLLLLLHLLLHHHHLHHHHHHHHHHHHHHHLHHHHHHH
   120  0101111111111111011  0HHHHHHHHHHHHHHH  LHLLLLLHLLLHHHHHLHHHHHHHHHHHHHHHLHHHHHHH
   135  1101111111111111011  0HHHHHHHHHHHHHHH  LHLLLLLHLLLHHHHHLHHHHHHHHHHHHHHHLHHHHHHH
   150  0101111111111111011  0HHHHHHHHHHHHHHH  LHLLLLLHLLLHHHHHLHHHHHHHHHHHHHHHLHHHHHHH
   165  1101111111111111011  0HHHHHHHHHHHHHHH  LHLLLLLHLLLHHHHHLHHHHHHHHHHHHHHHLHHHHHHH
   180  0101111111111111011  0HHHHHHHHHHHHHHH  LHLLLLLHLLLHHHHHLHHHHHHHHHHHHHHHLHHHHHHH
   195  1101111111111111011  0HHHHHHHHHHHHHHH  LHLLLLLHLLLHHHHHLHHHHHHHHHHHHHHHLHHHHHHH
   210  0101111111111111011  0HHHHHHHHHHHHHHH  LHLLLLLHLLLHHHHHLHHHHHHHHHHHHHHHLHHHHHHH
   225  1101111111111111011  1111111111111111  LHLLLLLHLLLHHHHHLHHHHHHHHHHHHHHHLHHHHHHH
   240  0101111111111111011  1111111111111111  LHLLLLLHLLLHHHHHLHHHHHHHHHHHHHHHLHHHHHHH
   255  1101111111111111011  1110000000001111  LHLLLLLHLLLHHHHHLHHHHHHHHHHHHHHHLHHHHHHH
   270  0101111111111111011  1100000000011111  LHLLLLLHLLLHHHHHLHHHHHHHHHHHHHHHLHHHHHHH
   285  1111111111111111011  1111110000000111  LHLLLLLHLLLHHHHHLHHHHHHHHHHHHHHHLHHHHHHH
   300  0111111111111111011  1111111111111111  LHLLLLLHLLLHHHHHLHHHHHHHHHHHHHHHHHHHHHHH
   315  1111111111111111011  1111111111111111  LLLLLLLLLLLLHHHHHHHHHHHHHHHHHHHHHHHHHHHH
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Figure 1 • Sample Vector File in NRZ Format

Figure 2 • Sample Logic Circuit

Figure 3 • Timing for Sample Logic Circuit

Hardware Constraints

If possible, at-speed simulation is recommended. Current Actel test equipment supports a range from 100 kHz (minimum) to about 75 MHz (maximum). The resolution in setting the tester period is currently 1 ns. This applies to all vector formats. In addition, there are other hardware constraints associated with particular vector formats as shown in Table 1.

Table 1 • Test Constraints

Parameter	Value	NRZ	RZ, RTO
Delay – min	0 ns	x	x
Delay – max	Cycle	x	x
Pulse Width – min	5 ns		x
Output Strobe Width – min	5 ns	x	x
Output Strobe Width – max	Cycle	x	x

Simultaneously-Switching Outputs (SSOs)

Noise voltages in text fixtures can sometimes be increased with large numbers of SSOs. To avoid triggering unintended device state changes, the number of SSOs in vector files should be minimized.

Conclusion

This application note describes a standardized test vector format that reduces cycle times and costs by simplifying design verification of Actel FPGAs on Actel test equipment. It is highly recommended that customers adopt this format for Actel parts.

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